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Development of Switched Capacitor based Single Phase Multilevel Inverter for Isolated Applications

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ABSTRACT

This work introduces a pulse width modulated (PWM) control approach for a single-phase, nine-level inverter suitable for use in stand-alone photovoltaic systems. To create the nine-level inverter, a single-phase conventional H-bridge inverter, three bidirectional switches, and four capacitor voltage dividers are suggested. The regulator signal is constructed from four reference signals with sinusoidal amplitudes that are as compared to a single triangle carrier signal used to regulate the inverter's switching. The inverter can produce nine different levels of output voltage, each of which is a more fundamental RMS output voltage with a less degree of THD. Results from a MATLAB simulation have validated the nine-level inverter that was suggested.

INTRODUCTION

Researchers in the area of power electronics are increasingly focused on renewable energy sources in response to rising energy demand and the fast depletion of non-renewable resources. Predictions indicate that the renewable energy source will provide us with useful energy for almost a millennium. And the renewable energy sources would lowers operational expenditures and emissions from fossil fuel consumption, therefore improving environmental conditions. One of the most common methods of producing electricity from sunlight, photovoltaic systems are becoming more widespread. Photovoltaic systems may be utilized for standalone purposes and feed their output into the grid Multilevel inverters are an advanced take on the traditional two-level inverter. The purpose of a single-phase inverter, whose basic design consists of four switches, is to produce a sinusoidal voltage from a variety of voltages, often those stored in capacitors. The primary advantage of this kind of inverter over a single switch with a higher VA rating is that current may be shared across numerous switches. In every other case, harmonics are permitted. The synthesized output waveform, which looks like a staircase, gets closer to the ideal waveform with diminishing harmonic distortion as the level count goes up Companies that provide high-power inverter systems have reported many distinct multilevel inverter topologies. Diode clamped, flying capacitor or multicell, cascaded H-bridge, and modified H-bridge multilevel inverter topologies are some of the most popular. The output from each of these three topologies is generated by a unique method. Clamping diodes and a series-connected capacitor are employed in the diode-clamped multilevel inverter, whereas floating capacitors and a series connection of H-bridges make up the cascaded kind. This diode-clamped multilayer inverter works by applying varying voltages across the inverter's various phases and, in turn, to the series-connected capacitor banks. Because of the low voltage it can transmit, diodes are often used to protect more sensitive electronic equipment. Diode clamped multilevel inverters have the disadvantage of being difficult to maintain, as the charging and discharging cycle becomes more taxing as the number of levels increases (as the number of diodes required increases quadratically). Adding more switches, diodes, and capacitors should solve the problem. Because of problems with balancing the capacitors, they can only be used on levels 1, 2, and 3. When using a power supply of the flying capacitor type, flying capacitors must be used in place of clamping diodes. Since flying capacitor multilevel inverters require switching redundancy within phase to balance the flying capacitors, their output is only half of the input dc voltage. Each H-bridge cell in the cascaded H-bridge multilevel inverter can generate a voltage of zero, a positive dc voltage, or a negative dc voltage. Compared to diode clamped and flying capacitor topologies, this one uses fewer parts. Each

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H-bridge cell should have its own dedicated dc supply. Multiple dc sources can cause voltage inconsistencies.

In section II, the paper proposes a novel modified single phase single source nine level inverter using a novel pulse width modulated scheme.

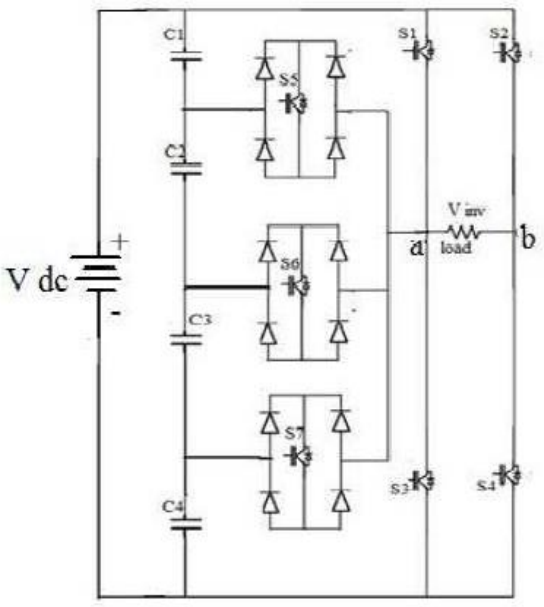
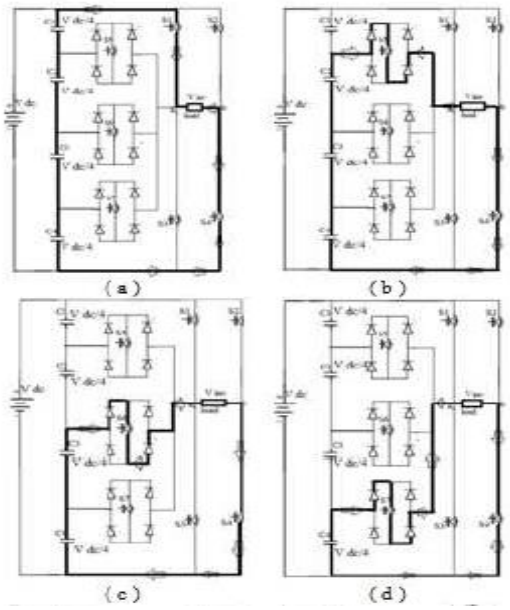


Fig. 1: *Power circuit diagram of proposed nine-level inverter.*

Put out a plan for nine tiers Single-phase conventional H-bridge inverter, three bidirectional switches, and four capacitor voltage dividers C1, C2, C3, and C4 make up the inverter's topology. H-bridge, abbr. Compared to diode clamped and flying capacitor multilevel inverter topologies, the advantages of the inverter topology are numerous, including a reduction in the number of components needed to produce an inverter with the same number of levels as its competitors, as well as a lower cost and lower overall weight. In this case, the isolated load is supposed to receive the power produced by the multilayer inverter. The suggested switching of the multilayer inverter uses a single dc source voltage to generate nine distinct levels of output voltage. There are nine possible output voltages: Vdc, 3Vdc/4, 2Vdc/4, Vdc/4, 0, -Vdc/4, -2Vdc/4, -3Vdc/4, -Vdc.

The expressions for the conducting modes are as follows:

Mode 1: $0 < \omega t < \theta_1$ and $\theta_6 < \omega t < \pi$
Mode 2: $\theta_1 < \omega t < \theta_2$ and $\theta_5 < \omega t < \theta_6$
Mode 3: $\theta_2 < \omega t < \theta_3$ and $\theta_4 < \omega t < \theta_5$
Mode 4: $\theta_3 < \omega t < \theta_4$
Mode 5: $\pi < \omega t < \theta_7$ and $\theta_{12} < \omega t < 2\pi$
Mode 6: $\theta_7 < \omega t < \theta_8$ and $\theta_{11} < \omega t < \theta_{12}$
Mode 7: $\theta_8 < \omega t < \theta_9$ and $\theta_{10} < \omega t < \theta_{11}$
Mode 8: $\theta_9 < \omega t < \theta_{10}$.



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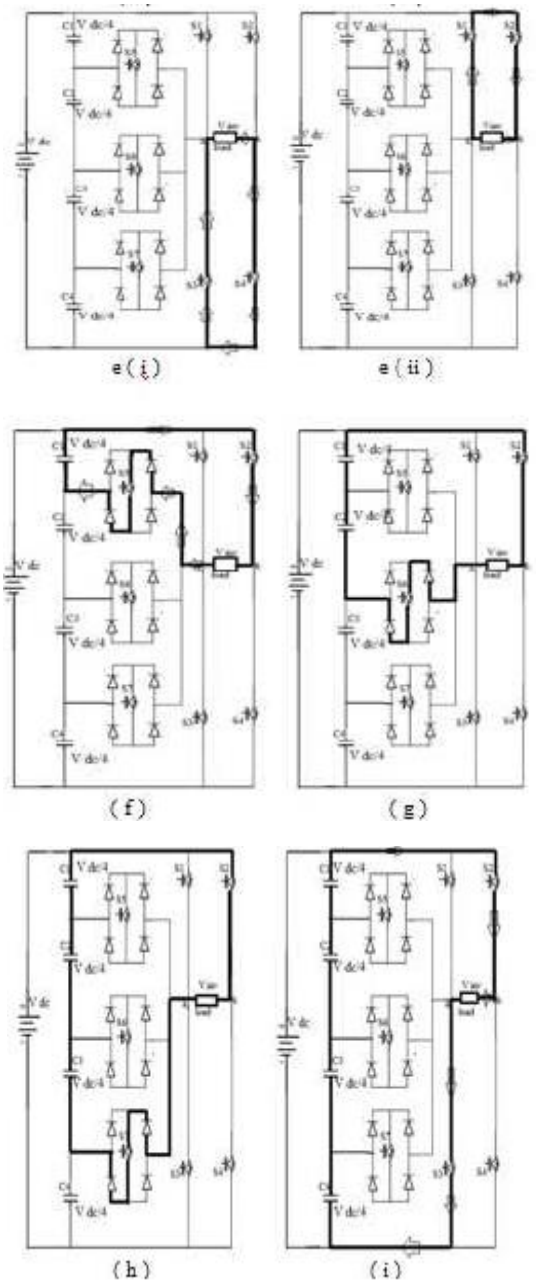

Fig. 2: *Different modes of operation of proposed nine level inverter (a)VA=Vdc, (b)VA=3Vdc/4, (c)VA=2Vdc/4, (d)VA=Vdc/4, e (I) and (ii) VA=0Vdc, (f) VA= -Vdc/4, (g)VA= -2Vdc/4, (h)VA= -3Vdc/4, (I)VA= -Vdc.*

Table 1: Output voltage according to the switches ON-OFF condition for nine-level inverter.

Inverter output voltage	Switching State combination						
	S_1	S_2	S_3	S_4	S_5	S_6	S_7
V_{dc}	1	0	0	1	0	0	0
$3V_{dc}/4$	0	0	0	1	1	0	0
$2V_{dc}/4$	0	0	0	1	0	1	0
$V_{dc}/4$	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
	1	1	0	0	0	0	0
$-V_{dc}/4$	0	1	0	0	1	0	0
$-2V_{dc}/4$	0	1	0	0	0	1	0
$-3V_{dc}/4$	0	1	0	0	0	0	1
$-V_{dc}$	0	1	1	0	0	0	0

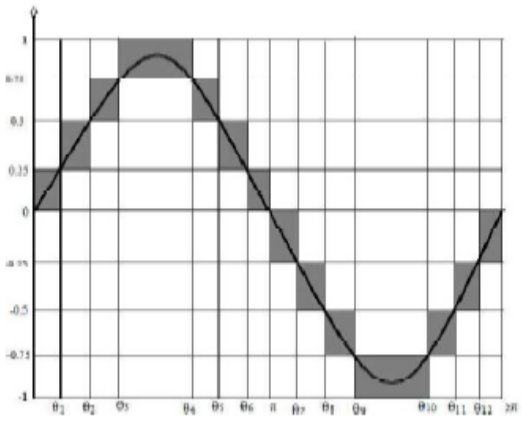

Fig. 3: *Output voltage and switching angles for nine level inverters.*

Mode 1: Maximum Positive Output Voltage (+Vdc): The switches S1 and S4 are conducting when this mode is activated. The current travels from S1 via the load and S4 before switching back to S1. The positive terminal of the load connects to Vdc while switch S1 is on, and the negative terminal connects to ground when switch S4 is on. Right now, just two switches are live. This leaves the remaining the switches are in the OFF position, therefore +Vdc is being supplied to the load terminal. The trajectory of this mode is shown in Figure 3(a). With the second setting, the bidirectional switch S5 and S4 conduct, producing a three-fourths positive output voltage (+3Vdc /4). Current flows from switch S4 to the load and back to switch S5 during this time. The load's positive terminal connects to Vdc while switch S5 is on, and the load's negative terminal connects to ground when switch S4 is on. In this moment, just two switches are active. Assuming that all other switches are also OFF, the voltage between the load terminals will be +3Vdc /4. The trending course of this mode is shown in Figure 3(b). Third, when the bidirectional switches S6 and S4 are in the "on"

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position, the output voltage is a quarter-of-a-volt positive (+2Vdc /4). At this time, power is routed through switch S4 and the load's bidirectional switch S6. The load's positive terminal connects to Vdc while switch S6 is on, and the load's negative terminal connects to ground when switch S4 is on. In this moment, just two switches are active. All other switches are OFF, thus the load terminals are receiving (+2Vdc /4). You may see where this mode is headed right now in Figure 3(c). In mode 4, the bidirectional switch between S7 and S4 conducts, resulting in a positive output voltage of +Vdc /4. At this time, the circuit consists of the load, switch S4, and the bidirectional switch S7. The positive terminal of the load connects to Vdc while switch S7 is on, and the negative terminal connects to ground when switch S4 is on. In this moment, just two switches are active. All other switches are OFF, thus the load terminals are receiving (+Vdc /4). This mode's expected future course is shown in Figure 3(d).

By conducting S5 and S2, Mode 5 generates an output voltage that is 1/4 as negative as the input voltage (-Vdc /4). Switch S2 is on, and electricity is flowing from the load via the bidirectional switch S5. S5's on position connects the positive terminal of the load to Vdc, whereas S2's on position connects the negative terminal of the load to Vdc. In this moment, just two switches are active. All other switches are closed, thus the load terminals are receiving a voltage of (-Vdc /4). The trending route of this mode is shown in Figure 3(f).

The bidirectional switch S6 and S2 conducts in Mode 6, which produces a negative two-fourths of a volt as the output voltage (-2Vdc / 4). The current goes from the load to Switch S2 and then back again via S6, the bidirectional switch. When switch S2 is on, the negative terminal of the load is connected to ground, and when switch S6 is on, the positive terminal of the load is connected to power. In this moment, just two switches are active. With all other switches in the OFF position, the voltage between the load terminals is (-2Vdc /4).

The trajectory of this mode at now is shown in Figure 3(g).

In Mode 7, the bidirectional switch between S7 and S2 is conducting, producing a -3Vdc / 4 negative output voltage. The current travels from switch S2 to the load and then back to switch S7 during this time. The positive terminal of the load is connected to power while switch S7 is on, and the negative terminal is connected to ground when switch S2 is on. In this moment, just two switches are active. All other switches are in the OFF position, and a voltage of (-3Vdc / 4) may be measured between the load terminals.

The trajectory of this mode at now is shown in Figure 3(h).

Maximum Negative Output Voltage (-Vdc) Mode 8 is activated by closing switches S2 and S3. All three switches, S2, S3, and the load are closed at this time. The negative load terminal connects to Vdc when switch S2 is on, and the positive load terminal connects to ground when switch S3 is on. In this moment, just two switches are active. All other switches are OFF, thus the load terminal is at a value of -Vdc. See its present trajectory in Figure 3(I).

III Development of PWM Scheme:

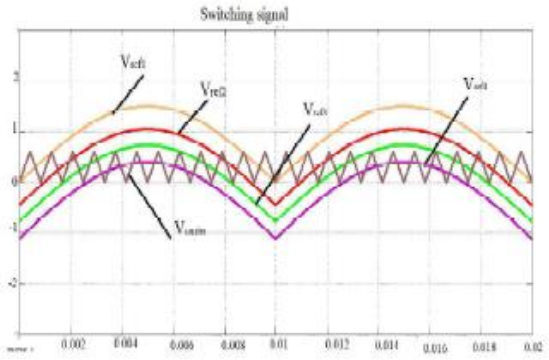

Fig. 4: *Single carrier and four sinusoidal reference signal.*

The PWM modulation system employs a high-frequency triangular carrier signal and a fundamental frequency reference signal consisting of four sinusoids. Figures 4 and 5 depict the production of the switching pattern used to regulate and generate the nine distinct inverter output voltage levels. Signals using pulse width modulation (PWM) for the switches of the inverter, a new method of PWM modulation was created. Specifically, the carrier signal was compared to four different sinusoidal reference signals (Vref1, Vref2, Vref3, and Vref4). If Vref1's amplitude was more than Carrier's peak amplitude, then Vref2's amplitude was compared to Carrier until the amplitude of the reference signal

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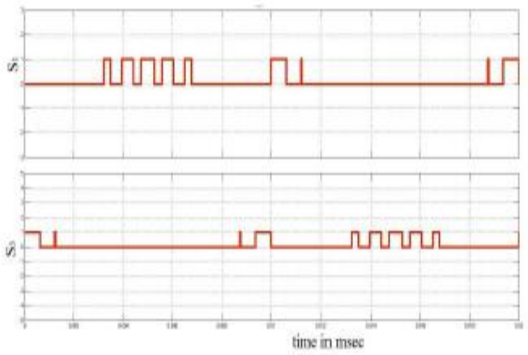
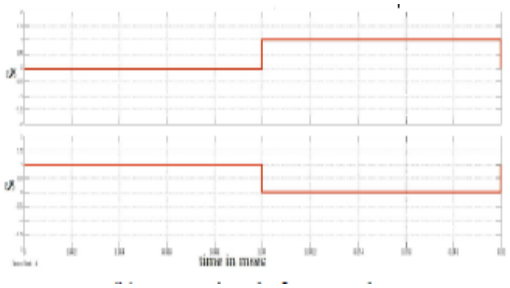
was greater than Carrier's peak amplitude. Then, until Vref3's amplitude equals the carrier signal, we would keep comparing the two. Once Vref3 had settled at zero, Vref2 would be compared to Carrier until Vref2 also settled at zero. Then, until Vref4's amplitude equals the carrier signal, we would keep comparing the two. When Vref4 equals zero, we'll start comparing Vref1 to Carrier until Vref1 equals zero. When the carrier signal is present, the S1, S3, S5, S6, and S7 switches will conduct at their respective rates, while the S2 and S4 switches will function at a frequency equal to the fundamental. After being adjusted, the inverter cycled through eight different conducting modes at the fundamental frequency.

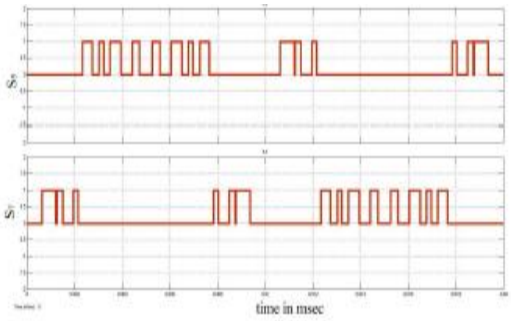
Modulation index Ma affects the numerical value of the phase angle. For a simple case of a reference signal and a carrier signal, we may theoretically define the modulation index as Ma = Am / Ac. To compare, the modulation index for a dual-reference signal and a single carrier signal is Ma = Am / 2Ac, while for a three-reference signal and a single carrier signal it is Ma = Am / 3Ac and for a four-reference signal and a single carrier signal it is Ma = Am /4Ac; the proposed nine-level inverter uses four-reference signals and a single carrier signal. When the modulation index is less than 0.25, the phase angle shift is negligible. defines 1 as 2 as 3 as 4 as 5 as 6 as /2 and 7 as 8 as 9 as 10 as 11 as 12 as 3 as /2. For modulation indices between 0.25 and 0.5, the phase angle displacement is defined as 1 = sin (/) ; 3 = 4 = /2 ; 6 = - 1 ; 7 = + 1 ; 9 = 10 = 3 /2 ; 12 = 2 - 1. The phase angle displacement is given by: 1 = sin (/); 2 = sin (2 /); 3 = sin (3 /); 5 = - 2 ; 7 = + 1 ; 8 = + 2 ; 11 = 2 - 2 ; 12 = 2 - 1. In the case where Ma is less than or equal to 0.25, only the lower reference signal (Vref4) is compared to the triangular carrier signal. The inverter operates similarly to a standard full-bridge, three-level pulse width modulation inverter. When Ma is between 0.25 and 0.5, the output voltage is a linear scale of five DC voltage levels, but only Vref2 and Vref3 reference signals are compared with the triangular carrier signal. Comparisons are made between the triangular carrier signal and the reference signals Vref3 and Vref4 for Ma values between 0.5 and 0.75. A total of seven different dc voltages may be pulled from the output. If the value of the modulation index is greater than 0.75, then nine distinct levels of output voltage will be generated. The inverter's switching signals are generated by comparing four sinusoidal reference signals with a single triangular carrier signal.



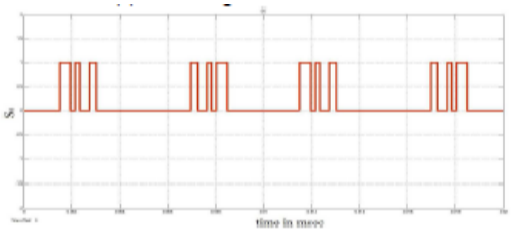
(a) ***PWM signals for S1 and S3***



(b) ***PWM signals for S2 and S4***



(c) ***PWM signals for S5 and S7***



(d) PWM signals for S6

Fig. 5: *Detail switching signal for the single-phase nine level inverter.*

IV Investigation of Proposed Inverter*:*

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Figure 6 depicts the Simulink model of the proposed single-phase nine-level inverter built using the pulse width modulation technique. One H-bridge, three bidirectional switches with embedded diodes, and four capacitor voltage dividers are required to create a nine-level inverter. In Fig.7, we can see the PWM switching generation of the nine-level inverter. The triangular carrier signal at high frequency should be compared to a reference signal consisting of four sinusoids at the base frequency. In an H-bridge, one leg of the switches operates at fundamental frequency while the other legs operate at high switching frequency.

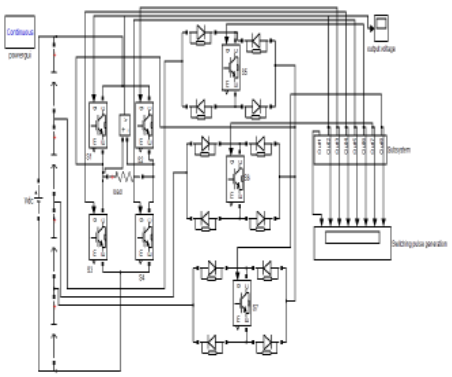

Fig. 6: Simulation of nine-level inverter.

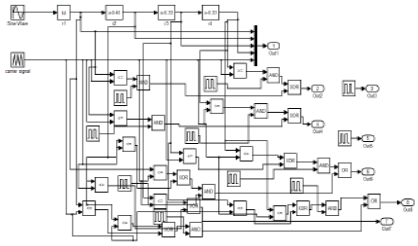

Fig. 7: Simulation of PWM switching generation.

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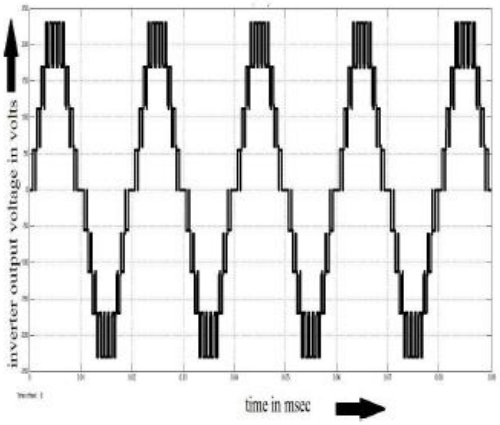

Fig. *8:* *Potential inverter voltage at the ninth level of the proposed circuit*.

Figure 8 displays the nine-level inverter's Viv output voltage simulation result. There are nine different voltage levels available from the inverter's output: 0 Vdc, Vdc/4, Vdc/3, Vdc/2, and Vdc/0. The results by changing the inverter's modulation index, the output voltage may be adjusted. As we've established, the output voltage varies throughout a spectrum defined by the modulation index.

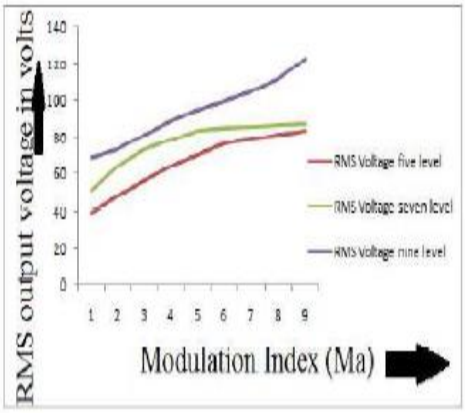

Fig. 9*:* *Modulation index versus root-mean-square output voltage.*

The relationship between the Modulation index and the RMS output voltage is graphically shown in Fig. 9. Based on this depiction, it seems that the RMS output voltage of a nine-level inverter is more than the five-level and seven-level inverter for single-

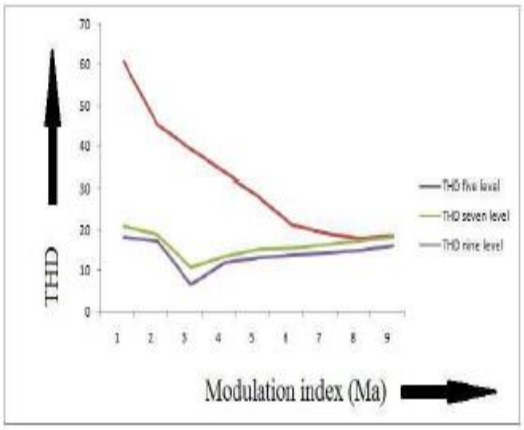

Fig. 10: Comparison of modulation index and THD.

Fig.10 shows the graphical representation of comparison between Modulation index and Total Harmonics
Distortion (THD) value. From this representation, the THD value of nine level inverter is decreased as compared to the five level and seven level inverters for the same value of Modulation index.

Conclusion:

In this work, we present the design and implementation of a nine-level inverter for use in completely self-contained Photovoltaic systems. The nine-level inverter has a brand-new PWM switching method. This simulation research has shown that the performance of a single-phase, DC-sourced device is inferior to that of a three-phase system.

A nine-level switched capacitor inverter has a low total harmonic distortion (THD) and a high fundamental rms output voltage over a wide range of modulation indices. The RMS output voltage and Total Harmonic Distortion (THD) values of a nine-level inverter are compared to those of a five-level and seven-level inverter. It finds that the nine-level inverter is an appealing option for renewable energy systems that operate independently.

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