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ENHANCED DELAY LOCKED LOOP BASED WIDE FREQUENCY MULTIPLIER

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Abstract
Design of clock generator circuit which generates multiple frequency clocks from reference clock is challenging as well as one of the most important task in digital system design. Digital circuit operates different speed it require multiple clocks .Digital circuit operates in different speed require clock with multiple frequency. Frequency multiplier is the circuit used in clock generator. General multiple frequency clocks are derived using frequency multiplier. A Phase locked loop(PLL) based frequency multiplier is the basic frequency multiplier circuit which has the limitation of are jitter accumulation and unstable output. Delay locked loop(DLL) based multiplier overcomes these limitations. Delay locked loop has major component in DLL based multiplier which produces multiphase clock. In this paper, Enhanced DLL(E-DLL) to produce 1,2,4,8,16,32 and 64 multiphase clock is proposed using voltage control delay line which reduce phase capture loss voltage. To maintain constant supply voltage, modified charge pump is used. The proposed delay locked loop is fabricated using a 90-µm CMOS process which increases multiplication ratio and produces output frequency range from 100 MHz -6.6 GHz . The frequency multiplier achieves power consumption to a frequency ratio of 17.4 µW/MHz

Keywords-- Frequency multiplier, phase detector, delay locked loop (DLL), low power, wide range

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INTRODUCTION

The clock generator is an essential circuit for digital system operation. Frequency multiplication is the key concept used in clock generator. There are many frequency multiplier circuits are in use, however designing wide frequency, low power, high speed frequency multiplier without jitter accumulation is a real challenge. Conventional, clock generators are implemented using a phase-locked loop (PLL) to produce multiple clock frequency.

PLL has Voltage controlled oscillator which produces variable frequency based on the error signal. Phase is integration of frequency hence order of the PLL is increased which increases delay accumulation. PLLs have some more limitations such as the difficulty of design, expensive loop filters, and accumulation of jitter. Hence recent clock generators are implemented using Delay-locked loops (DLLs). DLL uses a delay line instead of an oscillator, which can be used for generating multiphase clock from the reference clock. Frequency multiplier uses Edge combiner which combines both positive and negative edges of generated multiphase clocks. To generate different frequencies of various ranges, a controlled logic multiplication ratio is used.

The pulse generator gives the appropriate number of pulses from the multiphase clocks as per the controlled logic of multiplication, provides a multiplied clock by the generated pulses. The maximum multiplication ratio in frequency multiplier is half of its number of multiphase clocks. The locking time and the jitter performance are always the important consideration in the design of DLL. DLL based frequency multiplier produces the multiplied clock by gathering the multiphase clocks, hence multiplication ratio can be increased by increasing generation of multiphase clock. In this paper, low power, high speed wide frequency clock generator is proposed with enhanced DLL.

The paper is organized as, section II discusses related work, section III explains DLL based multiplier and section VI explains proposed enhanced DLL for wide frequency clock generator. In section V, simulation results are discussed and Section VI concludes the paper.

RELATED WORK

Power consumption is one of the major challenge in designing DLL based frequency multiplier hence authors of [1] proposed low power dual edge triggered flip flops. Locking range and frequency multiplication issues are rectified using phase detector with reset circuitry in [2].

Thomas D. Burd*et al*[3] proposed high throughput microcontroller system using dynamically varying clock generator using DLL based frequency multiplier. Programmable CMOS based DLL which can generate frequency in the range of 270 MHz to 2.4 GHz is proposed by Chuan-Yu Liu *et al* [4], however it produces more jitter.

Authors of [5] discussed multiphase clock generation using shift register instead of DLL, it increases circuit complexity and power consumption.

Jabeom Koo et al [6] proposed low power DLL but it has more delay and jitter accumulation. Authors of [7] proposed DLL based frequency synthesizer for wideband application, however it provides offset frequency of 1 MHz and above.

Shen-Iuan Liu*et al* [8] proposed DLL based multiplier to produce 40GHz clock using 90nm CMOS technology, however it consumes more power and needs improvement. It increases speed of DLL compared with conventional single edge triggered DLL.

Mohamed Elgebaly, *et al[9]* proposed frequency multiplier which maintains voltage level of output signal with the introduction of noise in frequency. In DLL based multiplier is flicker noise, hence Gang Luo *et al* [10] proposed improved VCDL line for reducing flicker noise.

This improved VCDLprovides 30 phase clock, however it decreases linearity and consumes more power. Dual edge triggered based DLL is proposed by authors of [11] for increase multiplication ratio. However the Dual edge triggered phase detector could be improved to reduce capture lock hence True

Single Phase Clock (TSPC) logic flip flop based dual edge triggered phase detector for high locking speed and less jitter is proposed by Prasanna Kumar. L *et al*[12].

Edge combiner design with control logic is proposed by authors of [13] to achieve high speed and wide frequency multiplication ratio, it also minimizes jitter. However, wide range and low power consumption could be achieved by modifying charge pump and dual phase detector circuit of DLL. In this paper enhanced DLL using modified charge pump and dual edge phase detector is proposed for high speed, low power wide range frequency multiplication.

DLL BASED FREQUENCY MULTIPLIER

The two major parts of DLL based frequency multiplier o is dual edge triggered phase detector delay locked loop and frequency multiplier as shown in Fig .1. Delay locked loop consists of dual edge triggered phase detector, charge pump, loop filter, voltage control delay line and delay element for generating multiphase clock. Generated multiphase clock from this unit is applied to frequency multiplier clock to generate frequency multiplied signal.

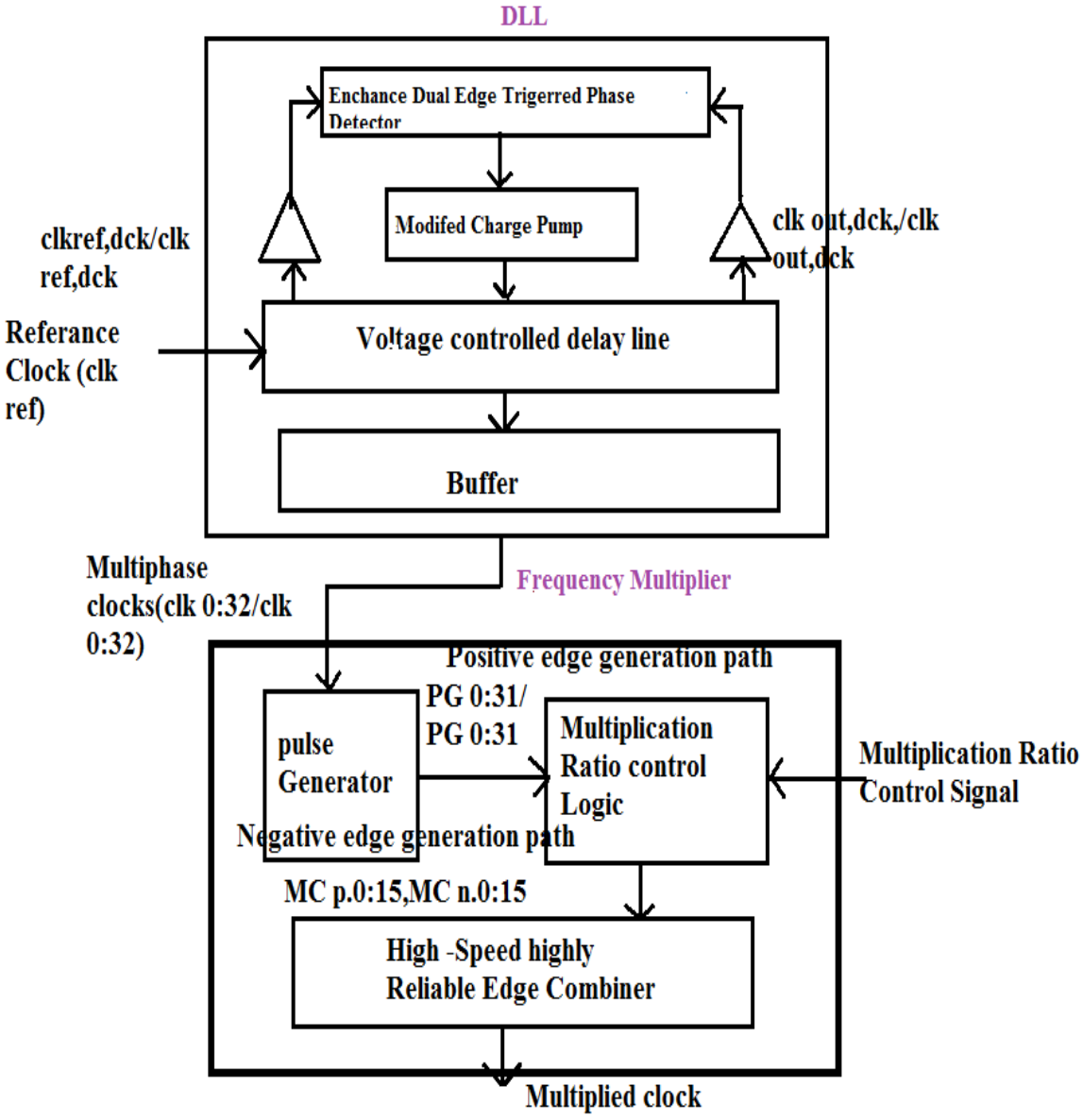

Figure 1. Block diagram of DLL based frequency multiplier

Enhanced DLL to obtain 64 phase clock by detecting positive and negative edge is proposed in this paper. It also reduces capture lock by introducing one more transistor.

ENHANCED –DLL BASED MULTIPLIER

A. Modified Dual Edge Triggered Phase Detector

Dual edge triggered phase detector comparing the signal at both positive and negative edges of reference signal and output of feedback signal is called edge triggered phase detector which reduces the power consumption in the clock distribution network. The schematic diagram of modified phase detector is shown in fig 2.

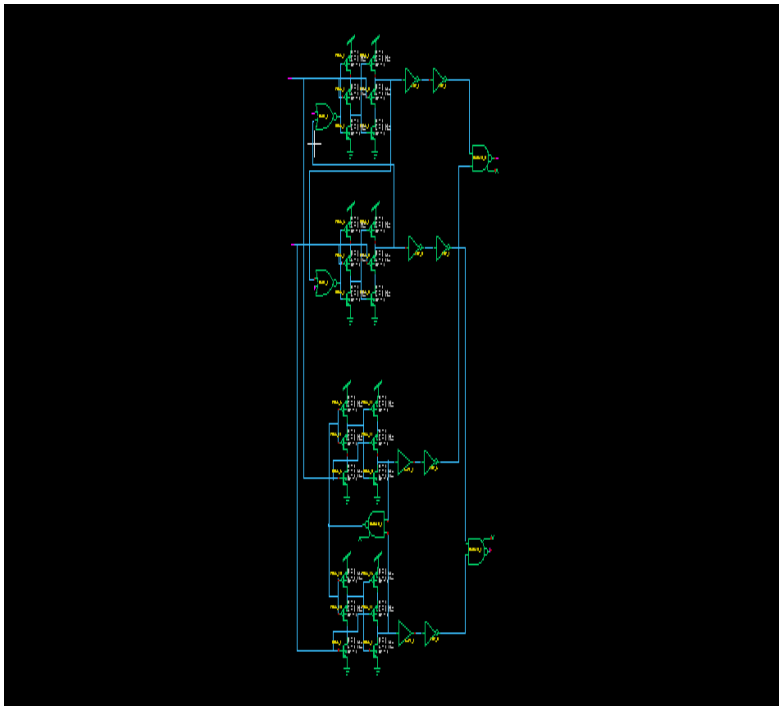

Figure 2. Schematic of modified Dual edge triggered phase detector

DLL can be classified into two types analog delay locked loop and digital delay locked loop, according to the method used to control the variable delay line. Digital DLL has static phase offset and clock jitter, analog DLL has higher locking time and loss of phase capture. Dual edge triggered phase detector has positive edge triggered phase detector to compare the result between the positive edge of the reference clock and that of the voltage controlled delay line (VCDL) output. It also uses negative edge triggered phase detector to produce comparison result between the negative edge of the reference clock and that of VCDL output. Final block combines output of positive and negative edge triggered phase detectors. In this work, the Positive edge triggered phase detector is replaced by modified True single phase logic phase detector(TSPC-PD), which reduces power consumption and increases speed. It provides constant output for the input phase difference ranges from $-\pi$ to π and ranges from -2π (π) to $-\pi$ (2π). In addition one NOR gate is used in the reset path of the conventional TSPC-PD, which results in loss of the phase capture range and reducing the locking speed. The negative edge triggered phase detector is reconstructed using PMOS and NMOS positions from the conventional TSPC-PD which improves overall performance of phase detector.

B. Charge pump

Design of charge pump is quiet tedious in DLL. There are two methods for designing charge pump. First method uses tri-state logic, when both signal are low, i.e both the MOSFETs are 'OFF' then the output is in a high impendence state. If the QA signal goes high, PMOS turns 'ON' and pulls the output to the VDD, if the QB is high, the output is pulled low through NMOS. The main problem of charge pump is power supply variation can significantly affect the output voltage when PMOS is ON.

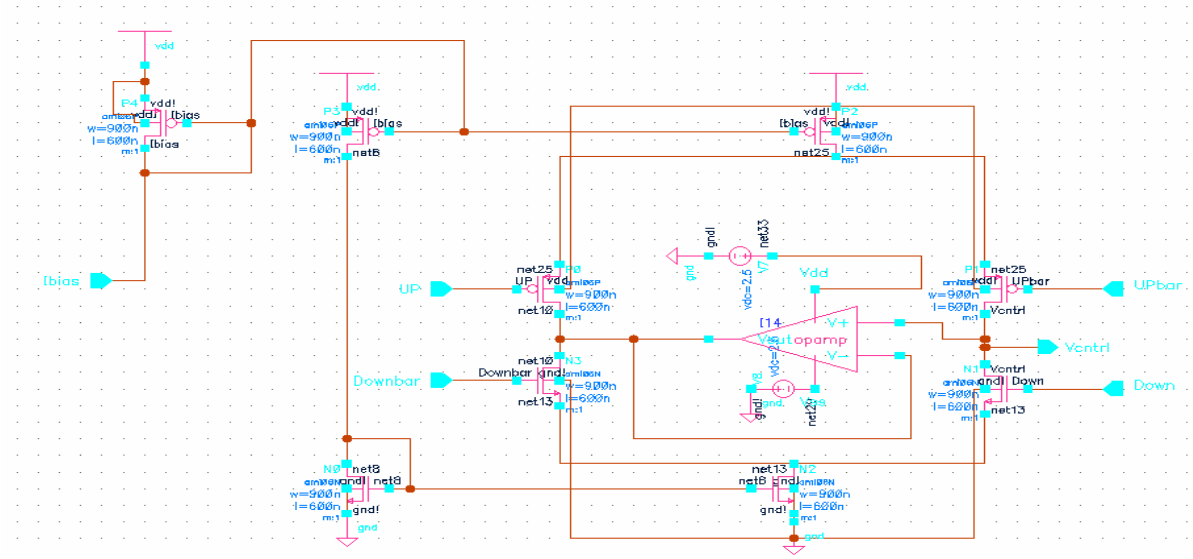

Figure 3. Charge pump

C. Modified Charge Pump

In modified charge pump single current source is replaced by two switched currents sources that charge into or out of loop filter according to two logical inputs. The circuit has three states and ensures that MOSFETs are in saturation. The charge pump consists of two switched current sources that pump charge into or out of the loop filter according to two logical inputs.

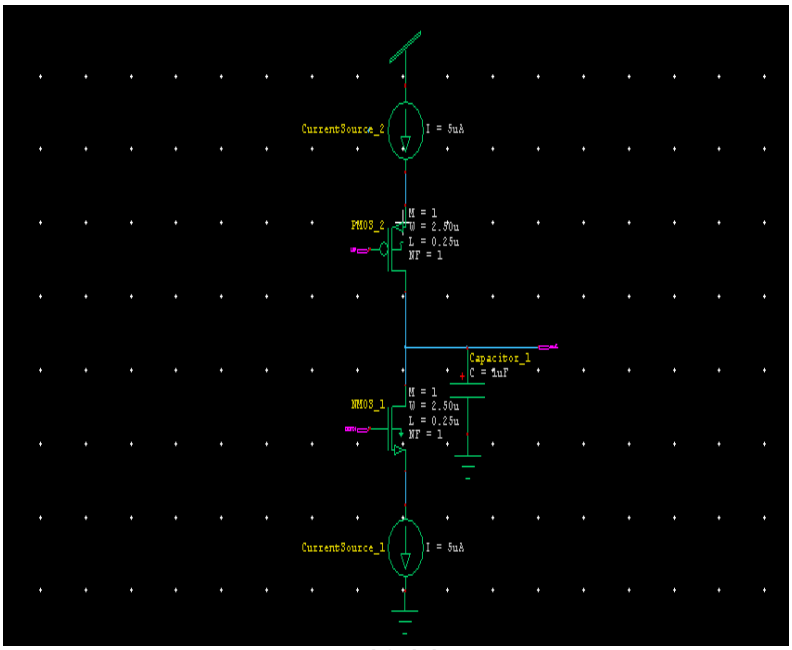

Figure 4. Modified charge pump

In modified charge pump when both the transistors are 'OFF' i.e QA= QB=0, then both switches are open and output voltage remains constant. If upper transistor is 'ON' and lower transistor is 'OFF', then current through the PMOS branch charges the capacitor. Conversely if upper transistor is 'OFF' and lower transistor is 'ON', then current through the PMOS branch discharges the capacitor.

Hence, whenever A leads B, then QA continues to produce pulses and output rises steadily and whenever, B leads A, then QB continues to produce pulses and output falls steadily. The currents through the PMOS branch and NMOS branch are nominally equal and power supply retains constant.

SIMULATION RESULTS AND DISCUSSION

The proposed Enhanced DLL based frequency multiplier with modified charge pump is verified with existing technology using tanner software. Table.1 shows the simulation parameter used for comparison

Table 1. Simulation Parameters

Parameters	Existing			PROPOSED-EDLL
PROCESS	0.35µm	0.13µm	180µm	90µm
VDD	3.3V	1.2V	1.1V	1.2V
Architecture	PLL+FM	PLL+FM	PLL	DLL+DLL
Overlap Cancel	X	X	N/A	0

Fig 5.shows multiphase clock generated from Enhanced DLL, which shows 64 phase clocks are generated in positive and negative edge. Fig. 6 shows the power analysis of the enhanced DLL based frequency multiplier, its inferred that power consumption is reduced to due to modification in dual edge detector and modified charge pump

Figs. 7 and 8 Show the lower and higher multiplication ratio output obtained from enhanced –DLL based multiplier. The overall performance improvement is given in table 2.

Table 2. Performance analysis

Parameters	PLL Based Multiplier	DLL based multiplier	Enhanced DLL based Multiplier
Maximum Multiplication Ratio	4	16	32
Output Range	120MHz-1.8 GHz	1.5 GHz	100MHz-6.6 GHz
Power frequency ratio of frequency multiplier of DLL	54 µW/MHz	11µW/MHz	17.4µW/MHz

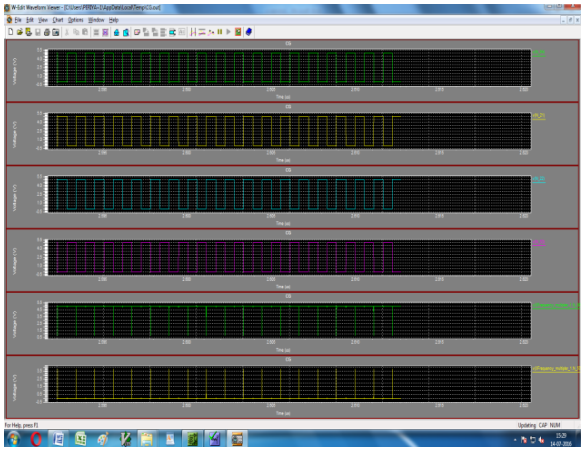

Figure 5. Generated Multiphase clock

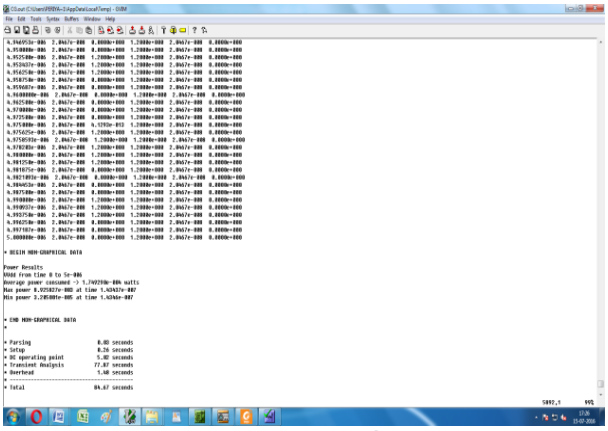

Figure 6. Power analysis

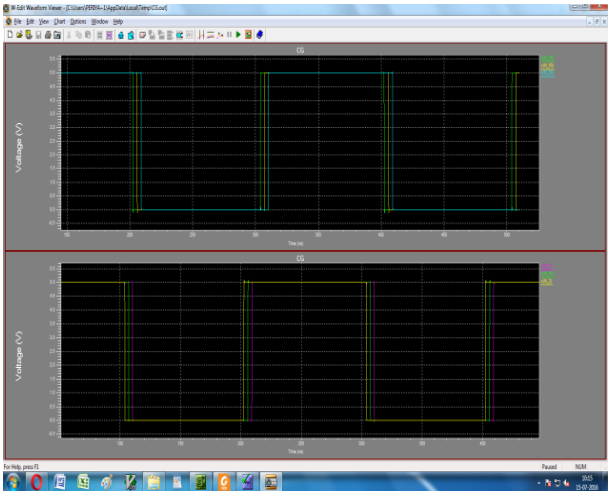

Figure 7. Output with low multiplication ratio

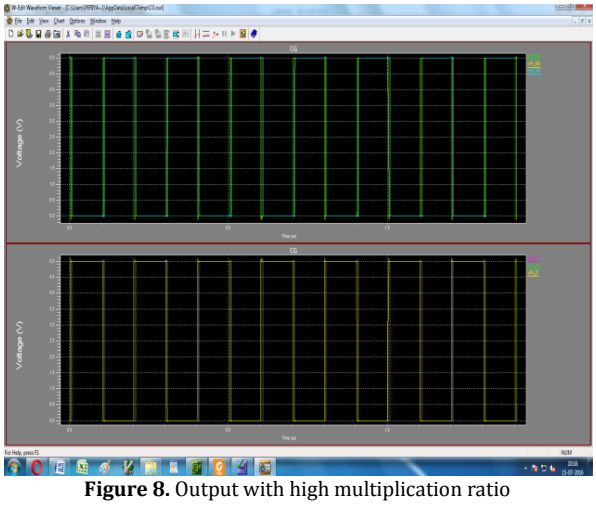

Figure 8. Output with high multiplication ratio

CONCLUSION

A wide frequency multiplier which can generate output frequency in the range 100 MHz–6.6 GHz using high-speed DLL-based clock generator withhierarchical structurewith overlap canceller has been proposed. The Efficient multiplication-ratio control logic and optimized pulse generator are used to reduce the delay difference between positive and negative edge generation paths. The proposed multiplier generates wide range of frequency with less power consumption.

REFERENCES

1. J. S. Wang, "A New True-Single-Phase- Clocked Double Edge Triggered Flip-Flop for Low-Power VLSI Design", Proceedings of IEEE International Symposium on Circuit and Systems, pp. 1896-1899, 2000
2. C. Kim, I-C. Hwang and S-M. Kang, "A low-power small-area±7.28-ps-jitter 1-GHz DLL-based clock generator," IEEE Journal. Solid-State Circuits, vol. 37, pp. 1414-1420, no.2, 2002
3. Thomas D. Burd, Pering, Anthony J. Stratakos," A Dynamic Voltage Scaled Microprocessor System", *IEEE Journal of solid-state circuits, vol. 35, no. 11,* 2004.[
4. Chuan-Yu Liu, Ro-Min Weng, Tung-Hui Su," A CMOS 2.4 GHz Delay-Locked Loop Based Programmable Frequency Multiplier", Vol. 29, pp. 1222 - 1223, 2004.
5. Xiang Gao, eric a.m. klumperink ," Low-Jitter Multi-phase Clock Generation a Comparison between DLLs and Shift Registers" IEEE Journal ,of Solid-State Circuits, vol. 31, pp. 2015 - 2023, 2005
6. Jabeom Koo, Sunghwa Ok and Chulwoo Kim, " DLL-Based Clock Generator With low power, low area Antiharmonic Lock" ," *IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1136-1140, 2006
7. Tai-Cheng Lee and K.-J. Hsiao, "The design and analysis of a DLL-based frequency synthesizer for UWB application," IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1245– 1252, 2006.
8. Chi-Nan Chuang and Shen-Iuan Liu, "A 40 GHz DLL-based clock generator in 180 nm CMOS technology," Proceedings of *IEEE International conference on Solid-State Circuit,* pp. 178–185, 2007
9. Mohamed Elgebalyand ManojSachdev, " Variation-aware adaptive voltage scaling system," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 5, pp. 560–571, 2010.
10. Gang Luo and XianjunZeng , "An Improved Voltage-Controlled Delay Line For Delay Locked Loops", Proceedings of IEEE international conference on Computer Research and Development , pp. 581–590, May. 2011
11. KyunghoRyu, Dong-Hoon Jung and Seong-Ook Jung, "A DLL with Dual Edge Triggered Phase Detector for Fast Lo ck and Low Jitter Clock Generator," *IEEE transactions on Circuits and Systems*, vol. 59, no. 9, pp. 1860-1870, 2012
12. Prasanna Kumar. L , Ashok. S and ArunKumar.N, " Dual Edge Triggered Phase Detector for DLL and PLL Applications**",**Int. Journal of Engineering Research and Applications, vol. 5, no.5, pp. 12-15, 2015
13. KyunghoRyu, Jiwan Jung, Dong-Hoon Jung, Jin Hyuk Kim, and Seong-Ook Jung' 'High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based clock generator," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no.04,pp.1484-1493, 2016

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