

FPGABASED AVANCED ERROR CORRECTION FOR FAILURE RECOVERY

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ABSTRACT: Parallel failure recovery and mean time between failures is very important for VLSI digital electronic circuits. Different fault tolerance mechanisms are available for designing a chip. But, they have some limitations, like: tolerance range, scatter/gather loading and data backup. The FFT (Fast Fourier Transforms) remain important components in several “communication” systems. The CMOS technology scaling is decreasing day by day. So, parallel processing is necessary, because of these faults occur. Parity checks available for parallel fault protection but did not solve some technical problems. In order to remove above conflicts introduced two models, i.e. 1st one is Automated Traditional Check with Plancherel Function is proposed for parallel fault tolerance. In addition to this (2nd method) artificial intelligent algorithmic based fault tolerance (AIABFT) method is used for error correction codes. The combination of two schemes ATCPF, AIABFT gives the design complexity reduction and protection for combination and signal processing system.

Keywords: Automated Traditional Check-Plancherel Function (ATCPF), Artificial Intelligent Algorithmic Based Fault Tolerance (AIABFT), Error correction codes, FFT.

1. Introduction

Soft core and hard core errors are warning to modern and digital electric circuits. In this trending scenario safety along side easy going core and hard core errors requires on behalf of various requests. Communications as well as signal processing schemes remain no exclusions to this trend. For particular applications, a stimulating choice is to use artificial intelligent algorithmic-based fault tolerance (AIABFT) methods that attempt to adventure the algorithmic belonging to best Analysis, identify in addition to accurate mistakes. Signal processing as well as communication requests are well suitable for AIABFT. FFT and a fixed of SOS (sum of squares) checks that procedure an E.C.C (error correction codes), provide the finest consequences in terms of execution difficulty but parallel failure recovery and mean time between failures is not covered.

In standing of mistake analysis, error security, mistake in still at ion testing shows that the AIABFT E.C.C structure container improve everything the mistakes that are unavailable of the acceptance range. In addition to AIABFT automated traditional check point method is introduced, it can cover all error detection and correction and problems which are mentioned below.

This overhead is unreasonable on behalf of some applications. Added methodology is to attempt to utilize the algorithmic belonging of the circuit to distinguish/right blunders. This is generally alluded to as calculation founded adaptation to internal failure (ABFT) [4]. This procedure can decrease the overhead essential to secure a circuit.

2. Literature Survey:

This covers the viable utilization of trustworthy electronic frameworks in the genuine business, for example, space, train regulator, also car control frameworks, as well as system servers/switches. The effect of discontinuous mistakes brought about by ecological radiation (neutrons as well as alpha particles) also EMI (Electro-Magnetic Interference) are presented composed through their greatest progressive countermeasures [1]. This article extensively examines delicate blunder affectability in present-day frameworks and shows it to be application subordinate. The exchange spreads ground-level radiation components that have the most genuine effect on circuit activity alongside the impact of innovation scaling on delicate blunder rates in memory and logic [2].

After an expansion in the development VLSI framework plan, the region is a significant angle. we can't endure the gigantic zone contemplations consequently causes the colossal event of the issues and disappointments which can't be recognized at planning and furthermore in

testing yet that presents at the ongoing activity conditions[3].

For these kind of VLSI sign processing models as those suggested for the FFT and QR factorization, a utilitarian level concurrent error identification scheme is shown. Some basic characteristics connected with these estimations are used to verify the accuracy of the figured yield values[4]. These frameworks' unwavering quality is now and on a more fundamental, also tolerant channel implementations are needed to issue. Over the years, numerous strategies contain been suggested that seek the framework and characteristics of the channels to achieve adaptation to inner failure. It enables increasingly complicated frameworks to consolidate countless channels as innovation scales.

Generally, apart of the channels operate in parallel in these unexpected structures, for example, by applying a comparable channel to different info signals. As of late, a fundamental method was provided that adventures the proximity of parallel channels to achieve adaptation to non-critical failure[5]. The systems depend on joining current ECC methodology through the conventional SOS check. The SOS checks are utilized to recognize and find the mistakes and a straightforward equality FFT is utilized for remedy. The recognition and area of the mistakes should be possible utilizing an SOS check for every FFT or on the other hand utilizing a lot of SOS watches that structure an ECC[6]. The method alluded to as algorithmic delicate mistake resilience (ASET), exploits low-intricity estimators of the principle DSP square to achieve dependable activity within the sight of delicate mistakes. Three particular ASET methods- spatial, fleeting also Spatio-worldly are presented[7].

This paper proposes delicate NMR that nontrivially expands NMR by deliberately misusing mistake insights brought about by Nanoscale ancient rarities so as to structure strong and vitality productive frameworks. As opposed to traditional NMR, delicate NMR utilizes Bayesian discovery procedures in the voter. Delicate voter calculations are gotten through streamlining of fitting application-mindful expense functions[8]. It is demonstrated that solitary a little overhead proportion, $O(2/\log_{sub} 2/N)$ of equipment, is required for the systems to acquire deficiency secure outcomes in the main plot. A tale information retry strategy is utilized to find the broken modules. Enormous round off mistakes can be identified and treated in a similar way as practical blunders. The retry strategy can likewise recognize the round off mistakes and practical blunders that are brought about by some physical failures[9]. Calculation based adaptation to internal failure (ABFT) is a low-overhead framework level adaptation to internal failure system. Numerous ABFT plans consume been projected in the earlier for quick Fourier change (FFT) systems. In this broadsheet, another ABFT plot for FFT systems is projected. We demonstrate that the innovative method keeps up the in elevation throughput of past plans, yet wants lesserequipment overhead as well as accomplishes advanced deficiency meet than past plans by J.Y. Jou et al. (1988) also D.I. Tao et al. (1990)[10].

The TMR, which triplicates the plan and adds casting a ballot rationale to address blunders, is ordinarily utilized. Nonetheless, it dramatically multiplies the territory and intensity of the circuit, something that may not be satisfactory in certain applications. Computerized channels are generally utilized in sign making in addition to communication frameworks. At times, the reliability of those frameworks is simple, also flaw tolerant channel implementations are necessary. As improvement scales, it empowers increasingly complex frameworks that fuse numerous filters[12]. OFDM might be joined with radiowire exhibits at the spreader and recipient to expand the decent variety gain in addition to additionally to upgrade the framework limit on time-differing and recurrence specific channels, bringing about a numerous information various yield (MIMO) configuration[13]. the examination interests are in the zone of computerized interchanges, MIMO-OFDM frameworks, various access, asset portion, and execution parts of advanced correspondence frameworks.

He is the creator of a few global IEEE meeting and diary papers and designer of various licenses identified with OFDM-MIMO systems[14]. Versatile Broadband: Including WiMAX and LTE gives a diagram of IP-OFDM innovation, initiating with cell and IP innovation for the uninitiated while giving an establishment to OFDM hypothesis and developing advancements, for example, WiMAX, LTE, and beyond[15].

In current sign handling circuits, it isn't unexpected to discover a few channels working in parallel. Proposed is a zone effective strategy to identify and address single blunders happening two by two parallel channels that have either similar information or a similar motivation reaction. The system utilizes an essential execution involved two autonomous channels and a

repetitive usage that offers input information between the two channels in order to distinguish and address errors [16]. As modernization scales, it authorizes increasingly complex frameworks that join many channels. In those mind-boggling frameworks, usually, a portion of the channels work in equivalent, for example, through applying a similar frequency to numerous information signals. As of late, a straight-forward system that adventures the nearness of similar channels to achieve variation to internal failure has remained presented [17].

THE creator was directed to the examination given in this paper from a thought of enormous scale registering machines in which countless tasks must be performed without a solitary mistake at the last outcome. This issue of "doing things appropriate" on a huge scale isn't basically new; in a phone focal office, for instance, an enormous number of tasks are performed while the blunders prompting incorrectly numbers are monitored well, however they have not been totally disposed of. This has been accomplished, to a limited extent, using self-checking circuits [18].

Sign handling and correspondence frameworks are extensively utilized by Digital FFTs. This makes security contrary to delicate blunders a condition for different applications. For a couple of fuses, an energizing determination is to use algorithmically - based adjustment to non-basic disappointment (ABFT) frameworks that attempt to use the algorithmic properties to recognize an exact error. One point of reference is a quick Fourier change (FFT) that zone unit information structured during a couple of systems. Various thriving plans contain intended to recognize and bonafide botches in FFTs [19].

3.1 PARALLEL FFT PROTECTION USING ECCS

The assessment of the ECC methodology aimed at the security of similar FFTs shows its efficacy in aspects of overhead as well as security usefulness by proposing a new way founded on the usage of Parseval or Sum of Squares (SOSs) checks [4] paired through FFT parity. The suggestion for a fresh technique that uses the ECC on the SOS controls rather than on the FFTs

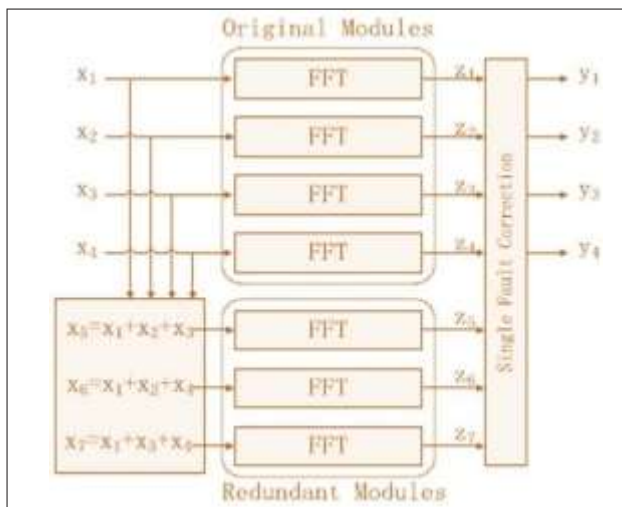


Figure :SOSmodel

The two proposed systems given new choices to ensure corresponding FFTs that container be additional proficient than securing everyone of the FFTs freely. The projected

plans have remained assessed utilizing FPGA usage to evaluate the security overhead. The outcomes demonstrate that by consolidating the utilization of ECCs also Parseval checks, the assurance overhead container be decreased contrasted and the utilization of just ECCs as planned in [17]. Flaw in fusion investigations have likewise been directed to confirm the capacity of the user to identify also address mistakes. The beginning stage aimed at our effort is the assurance plan dependent on the utilization of ECCs that was introduced in [17] for advanced channels. This plan has appeared in Fig. 1. In this model, a basic single mistake amendment Hamming code [18] is utilized.

In this work HJB based FFT model has been proposed for detecting the errors in Fast Fourier Transform (FFT). In modern communication this type of FFT error correction and detection gives the efficient results [19]. The first framework comprises of four FFT modules and three excess modules are added to distinguish and address mistakes. The contributions to the three excess

modules are straight blends of the sources of info and they are utilized to check direct mixes of the yields. For instance, the contribution to the primary repetitive module is

$$x_F \quad \text{eq(1)}$$

And subsequently the DFT is a linear operation, its output z_5 can be used to check that

$$z_F = z_1 + z_2 + z_3 \dots \text{Eq-2}$$

This will be meant as c_1 check. Similar thinking applies to the next two excess modules that will give checks c_2 and c_3 . In light of the distinctions seen on every one of the checks, the module on which the blunder has happened can be resolved. The various examples and the relating mistakes are abridged in Table I. When the module in mistake is known, the blunder can be adjusted by remaking its yield utilizing the rest of the modules. For instance, for a blunder influencing z_1 , this should be possible as per:

$$Z_1 c[n] = z_5[n] - z_2[n] - z_3[n] \dots \text{eq-3}$$

Comparable amendment conditions can be utilized to address mistakes on different modules. Further developed ECC can be utilized to address blunders on various modules if that is required in a given application. The overhead of this procedure, as talked about in [17], is lower than TMR as the quantity of repetitive FFTs is identified with the logarithm of the quantity of unique FFTs. For instance, to ensure four FFTs, three excess FFTs are required, however to secure eleven, the quantity of repetitive FFTs is just four.

This shows how the overhead diminishes with the quantity of FFTs. The above method will solve the error correction and detection schemes but fails parallel failure recovery and mean-time-between-failure shown in eq-1, 2 & 3.

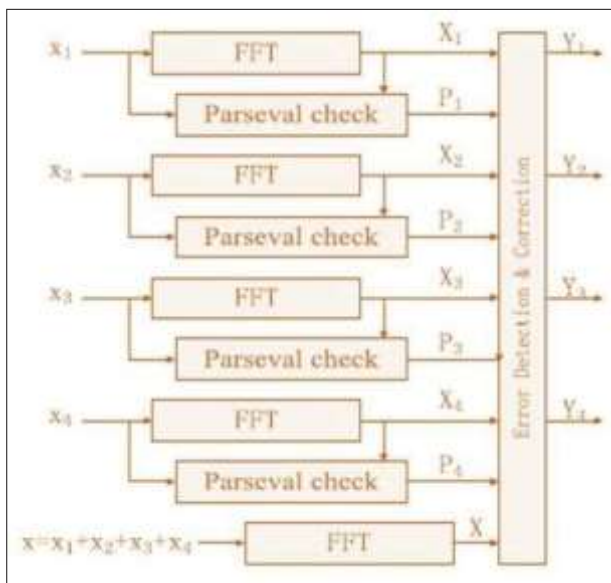


Figure : 2FFT summing operation

Scientists have planned two better strategies for checkpointing, diskless checkpointing [4][5] also application-level checkpointing [6][7]. Diskless checkpointing expands the speed of perusing or composing checkpoints by sparing them to recollection rather than the circle. Such a system is constrained by the space of memory. Application-level checkpointing gives the chance to the software engineer to pick the hour of checkpointing and spare the base measure of information important to recoup the program state. Be that as it may, these two upgrades together need the enduring procedures, composed through the bombed one, to move back upon recuperation, in addition to re-

try the undertaking flanked by the last checkpoint also the disappointment. This isn't proficient.

An epic adaptation to internal failure approach dependent on parallel disappointment recuperation called adaptation on non-critical failure parallel calculation (FTPA for short) [8]. While individual of the procedures that are implementing a similar program fizzes, FTPA utilizes all the enduring procedures to recompute the assignment missing by the bombed procedure, to quicken the disappointment recuperation. In this broadsheet, we talk about the plan and usage of the issue tolerant similar FFT utilizing FTPA in detail. We likewise study the number of procedures that partake in the parallel disappointment recuperation. A scientific model is projected to upgrade the exhibition of the flaw tolerant parallel FFT. At long last, we provide the investigation also assessment of the flaw tolerant equivalent FFT.

3.2 The fault tolerance parallel algorithm using parallel failure recovery

The adaptation to internal failure parallel calculation dependent on parallel disappointment recuperation is a novel adaptation to a non-critical failure approach [8]. It shares something for all intents and purpose with checkpointing. That is, the variation on non-critical failure parallel calculation needs to spare the middle of the road status at the specific focuses over the span of the program's execution. Be that as it may, contrasts exist. Upon a disappointment, the adaptation on non-critical failure parallel calculation does not require the move back of every enduring procedure. Rather, it grips their impermanent advances also usages them to figure the errand of the bombed procedure in similar. This determination diminishes the extra overhead brought about by adaptation on non-critical failure. After the disappointment recuperation, the enduring procedures are allowed to go on their executions.

At particular assumed focuses, every procedure in the calculation spares their calculation express, that is, that information required in the resulting calculation. The information of one procedure is sent to its neighbor for sparing. In a program, there may remain a few sparing focuses on its entire execution. These focus to separate the program hooked on a progression of segments. So we call the calculation flanked by 2 adjoining sparing focuses a 'square'. Toward the part of the bargain, I.e., just earlier than subsequent sparing point, there is a disappointment finder. On the off chance that a procedure is identified to be fizzled, other enduring procedures hold their current implementations. At that point, the procedure that holds the latest spared status information of the bombed one disperses the information also allotment the assignment of the bombed individual amongst the survivors. Furthermore, last, the survivors implement the errand shipped to them separately

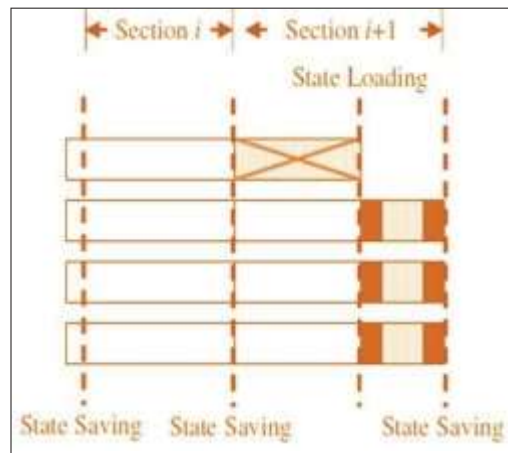


Figure:3 Parallel failure recovery

4. Design Methodology

Above all existed methods are not efficient methods compared to proposed Automated Traditional Check-Plancherel Function (ATCPF), Artificial Intelligent Algorithmic Based Fault Tolerance (AIABFT). Existed methods faces different problems like PFR and MTBF, these soft and hard problems are solved by our proposed method i.e. ATCPF, AIABFT.

4.1 Problem Finding:

1. parallel failure recovery (PFR) is not covered in this existed method
2. mean-time-between-failure (MTBF) is observed, not covered yet

The above two problems are not solved by the existed methods also did not efficient

4.2 Problem Solution

Automated traditional checkpoint method, AIABFT methods.

4.3 Plancherel's Theorem

The theorem of Plancherel states that perhaps the integral of As instances we container recollection the Fourier increases of min² also Maj³:

$$\min^2(x) = -12 + 12x_1 + 12x_2 + 12x_1x_2, \text{Maj}^3(x) = 12x_1 + 12x_2 + 12x_3 - 12x_1x_2x_3.$$

In mutually belonging the sum of squares of Fourier coefficients is $4 \times (1/4) = 1$.

In addition, generally assumed 2 functions $f, g: \{-1, 1\}^n \rightarrow \mathbb{R}$, we may calculate it by having to take the "dot product" of their coordinates in the orthonormal parity base. The following formula is named the theorem of Plancherel..

$$\langle f, g \rangle = \left\langle \sum_{S \subseteq [n]} \hat{f}(S) \chi_S, \sum_{T \subseteq [n]} \hat{g}(T) \chi_T \right\rangle$$

$$= \sum_{S, T \subseteq [n]} \hat{f}(S) \hat{g}(T) \langle \chi_S, \chi_T \rangle = \sum_{S \subseteq [n]} \hat{f}(S) \hat{g}(S)$$

...eq(5)

The disappointment of parallel controllers is analyzed considering the disappointment methods of squares. A technique for exploring the impact of joint modules disappointment on the power/minute capacities of a function's squared module is identical to the integral of its spectrum's squared module. It relates to the Fourier series theorem of Parseval. It is also always regarded as the theory of Rayleigh.

$$\langle f, g \rangle = \mathbf{E}_{\mathbf{x} \sim \{-1, 1\}^n} [f(\mathbf{x})g(\mathbf{x})] = \sum_{S \subseteq [n]} \hat{f}(S) \hat{g}(S)$$

eq (4)

controllers is introduced, and the criteria for full and incomplete recuperation from these disappointments are built up. The projected procedure is useable for together communication and signal processing equivalent processors; in the situation study as well as replication, FFT processors remain used as an instance.

$$\int_{-\infty}^{\infty} |E(t)|^2 dt = \int_{-\infty}^{\infty} E(t) \bar{E}(t) dt$$

$$\begin{aligned} &= \int_{-\infty}^{\infty} \left[\int_{-\infty}^{\infty} E_v e^{-2\pi i v t} dv \int_{-\infty}^{\infty} \bar{E}_{v'} e^{2\pi i v' t} dv' \right] dt \\ &= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E_v \bar{E}_{v'} e^{2\pi i t(v'-v)} dv dv' dt \\ &= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E_v \bar{E}_{v'} e^{2\pi i t(v'-v)} dt dv dv' \\ &= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \delta(v' - v) E_v \bar{E}_{v'} dv dv' \\ &= \int_{-\infty}^{\infty} E_v \bar{E}_v dv \\ &= \int_{-\infty}^{\infty} |E_v|^2 dv. \end{aligned}$$

----eq(6)

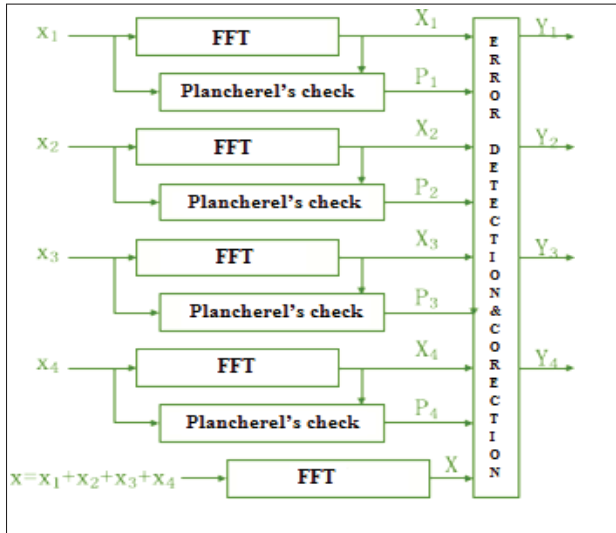


Figure:6 Automated traditional checkpoint

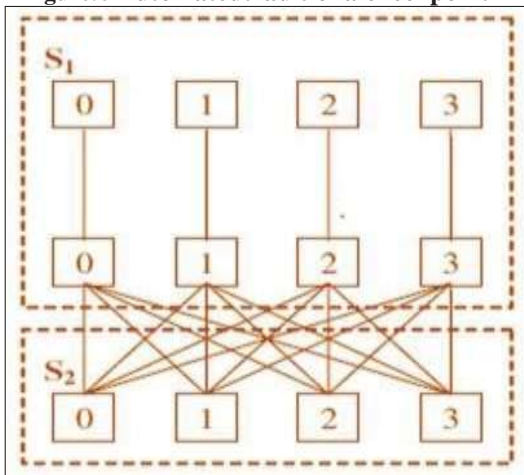


Figure:4 data recovery block

Along these lines, we can take the time overhead of these two sorts of tasks into two sections, to be specific information arranging time and information move time. The information sorting out time is identified with the number of procedure that partake in. The bigger the figure is, the advanced the overhead is. In any case, in the event that we deliberate the correspondence arrange as balanced in topology, the information move time determination be nothing to do through the areas of conveying gatherings, also just remain influenced through the measure of the information presence moved appeared in fig.4

$$X(n) = Y(n) \text{ where } X(n) \text{ is the Input, } Y(n) \text{ is the output.}$$

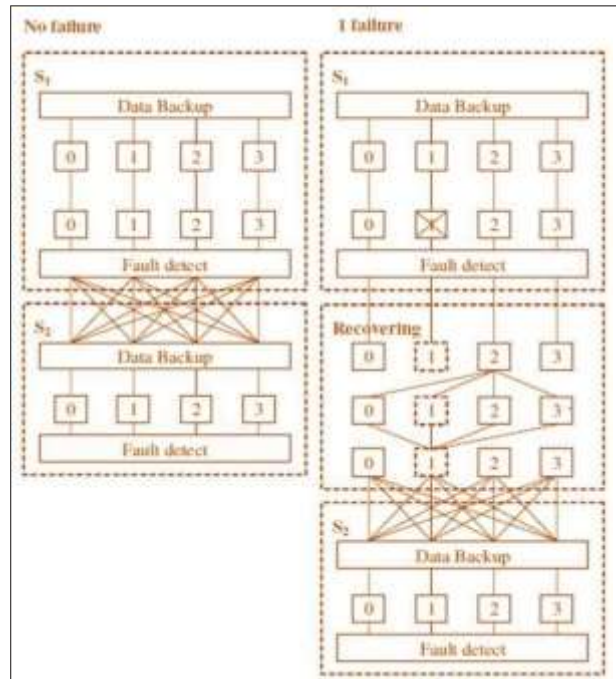


Figure: 5 complete faults detection and parallel failure recovery block

At the passage of each square, one needs to spare the factors whose definitions can arrive at the section. In the event that a disappointment happens, the disappointment recuperation needs to utilize these factors as its info. Toward the part of the bargain, there will be a disappointment identification, to check whether the procedure comes up short. With disappointment discovery, one procedure's disappointment can be known by all the enduring procedures. Upon the disappointment, all the enduring procedures, before proceeding with their own incomplete occupations, will take an interest in the disappointment recuperation, through re-computing the undertaking misplaced through the bombed procedure inequivalent. NPB-FT with similar disappointment recuperation appeared in fig.5.

Multiple-instruction-multiple-data (MIMD) notwithstanding guidance level parallelism from pipelining, a few processors can issue more than one guidance at once. These are known as superscalar processors. Guidelines can be assembled just if there is no information reliance between them. Score boarding and the Tomasulo calculation (which is like score boarding however utilizes register renaming) are two of the most widely recognized procedures for actualizing out-of-request execution and guidance level appeared in fig.6.

Complete parallel disappointment recuperation is practiced by three stages, disseminate the information, register in similar, also accumulate the outcomes. The first as well as third steps include correspondence. At the point when procedure number builds, time spends on registering will diminish, while that spent on dispersing and assembling may expand due to the steady correspondence tasks.

So we need to make an exchange off. Information dispersing incorporates information dividing and sending, while at the same time assembling is finished by accepting and consolidating.

RESULTS

We can see from the assumes that test results coordinate the hypothetical ends. At the point while the program keeps running on 64 as well as 512 procedures, utilizing 4 of them to do equivalent disappointment recuperation is ideal, although in the 128 procedures case, 2 procedures are right. We container like wi

se observethat in the composition of the directly above, the level of dispersing also assembling increments altogether through the digit of procedures that take an interest in the similar disappointment recuperation develops. Such an addition wipes out the benefits of parallelization also thusly turns the pattern of equivalent disappointment recuperation overhead starting plummeting to augmentation appeared in FIG.7

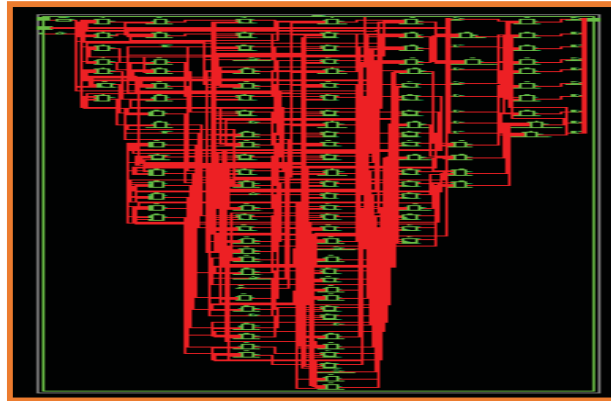


Figure:7 Automated traditional checkpoint method

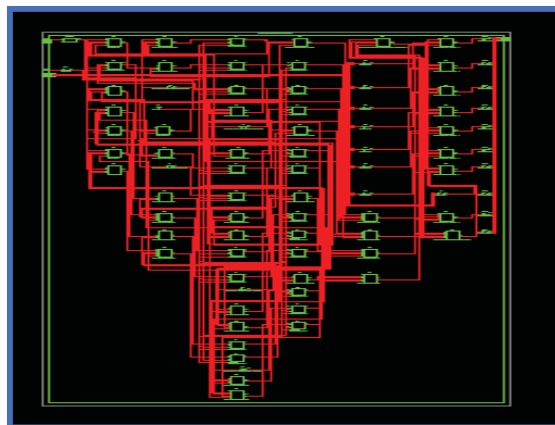


Figure:8 AIABFT

Fig.8 explains that AIABFT RTL schematic using this module removes the DSP problems, with the help of FFT removes parallel failure and mean time between failure is rectified.

Device Utilization Summary (estimated values) [1]			
Logic Utilization	Used	Available	Utilization
Number of Slices	39	5472	0%
Number of Slice Flip Flops	42	10944	0%
Number of 4 input LUTs	82	10944	0%
Number of bonded IOBs	20	240	8%
Number of GCLKs	1	32	3%

Table.2 belongs to area analysis of proposed system in this slices flip flops and luts are analysed.

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	42	10,944	1%
Number of 4 input LUTs	72	10,944	1%
Number of occupied Slices	50	5,472	1%
Slices containing only related logic	50	50	100%
Slices containing unrelated logic	0	50	0%
Total Number of 4 input LUTs	72	10,944	1%
Number of bonded IOBs	20	240	8%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFPGs	1		
Average Fanout of Non-Clock Nets	3.26		

Table:3detailedanalysis

	UN protected FFTs	ECC protected	Parity SOS-protected	Parity SOS-ECC protected	ATCPF, AIABFT
slices	15037	21811	23378	20156	5472
FFs	11407	16533	14727	13648	10944
LUT4	27830	40805	44273	38528	10944

Table_411PARALLELFFTcomparisonofperformance

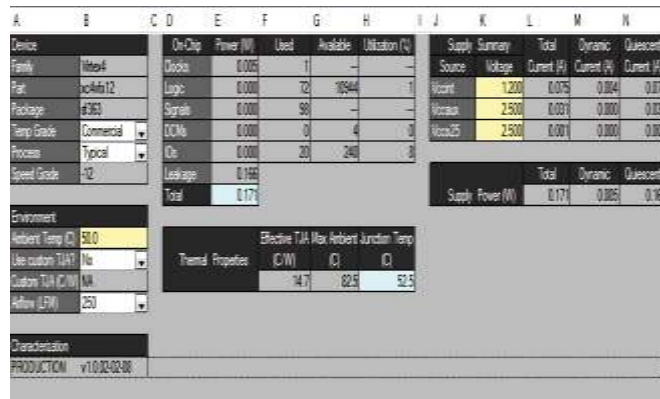


Figure:10poweranalysis

CONCLUSION:

As the consistently expanding size of elite parallelPC frameworks and multifaceted nature of VLSI, equipmentconstancy drops, thus ensures the MTBF. Enormous scalelogical requestscontainer barely run accurately deprived ofthehelpofadaptation tonon-criticalfailureinstruments. Alongtheselines, individualsare recurrently increasinglyphippingawayatadaptation tonon-critical failureissue. Plancherel'sCheckpointing is currently a generally utilizedrollback/restartinnovationforadaptationtonon-criticalfailure. It intermittently spares calculation state as well asburdensitupondisappointmentstorecouptheimplementation. Toexpandstatesparingalso

disappointment recuperation, Plancherel's checkpointing and application-level checkpointing have been proposed. Compared to the existing system, the proposed method gives the reduction of complexity of power and area and also removes the mean time between failure and parallel failure.

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