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IMPLEMENTATION OF FULL ADDER USING FINFET TECHNOLOGY WITH H-SPICE

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ABSTRACT

This study focuses on the simulation and comparison of different dynamic logic circuits, followed by the proposal of a circuit to reduce power consumption. Through our investigation, we observed a significant reduction in power consumption and lower delays by employing the proposed buffer circuit.

Furthermore, we explored the application of Gate Diffusion Input (GDI) techniques in the design of logic circuits. Specifically, we utilized GDI techniques to design logic circuits such as AND, OR, XOR, and multiplexers. Our findings revealed that this technique allows for the design of logic circuits with a reduced number of transistors.

In addition, we addressed the design of a collector circuit using the GDI technique and presented a collector circuit implemented with this approach. Based on our analysis, we concluded that the proposed circuit exhibits considerably lower delay and power consumption compared to previous works.

Overall, this study involves the simulation and comparison of various dynamic logic circuits, introduces a circuit for power consumption reduction, explores the utilization of GDI techniques in logic circuit design, and presents a collector circuit using this technique. Our results demonstrate the superior performance of the proposed circuit in terms of reduced delay and power consumption when compared to existing approaches.

Keywords: Gate Diffusion Input, XOR, XNOR, Simulation.

1. INTRODUCTION

1.1 Overview

An increase in the level of integration in modern Very Large-Scale Integration (VLSI) technology has rendered possible integration of many complex components in a single chip. Moreover, an analog circuit technique in the front-end wireless communication demands a digital domain to save power. In most of these applications, multipliers have been an obligatory component and determine overall circuit performance with respect to speed, power consumption and size. Hence, the goal of this research work is formulated to design an Arithmetic and Logic Unit (Full Adder) with less delay, low power consumption and compact area. In general, the performance of Full Adder in terms of delay, power consumption and area can be improved by two methods.

First one is based on efficient implementation of Full Adder function, whereas another relies on proper selection of logic style for its implementation. There have been various multiplication methods for realizing the low power and high-speed Full Adder introduced in the last few decades. However, in these multiplication techniques, the intermediate computation involved in the Full Adder operation reduces the speed exponentially in accordance with the width of the Full Adder input bit. This becomes a critical issue for a higher number of input bits. But this issue can be mitigated by the addition of partial products in parallel, which is adopted from mathematics-based multiplication. Hence, these 2 works explores possible techniques on an existing Full Adder for better performance.

As stated earlier, the logic styles used for realizing the multipliers have significant influence on the speed, size, power consumption and wiring complexity. Numerous logic styles in the classes of static Complementary Metal Oxide Semiconductor (CMOS), dynamic, transmission gate, Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) logic are discussed in the literature. Among them, GDI is considered in this research work due to its merits of low power consumption and implementation of any functions with low transistor count. However, the gates based on this logic suffer from a low output voltage due to the threshold voltage drop. This has motivated us to propose an improved set of gates that operate with merits of full swing without increasing the fabrication complexity with the possibility of implementing with less transistor count.

Based on these gates and adders in mind, new compressors and parallel adders shall be designed. Further, the Full Adder shall also be realized with the help of these designs.

The objectives of the research work are listed as follows:

- To propose the gates namely, AND, OR, XOR and XNOR with full swing GDI logic and to extend the designed gates for implementing the full adder designs.
- To improve the performance of parallel adders by implementing them using aforementioned full swing GDI gates and adder
- To propose Full Adder architecture with less delay, low power consumption and small area using the concepts with full swing GDI logic

2. LITERATURE SURVEY

An extensive literature survey is being carried out in order to confirm the need for the proposed objective. Initially, the reason for selection of GDI logic and its bottlenecks are explained, and then the full swing mechanisms available in the literature for GDI logic are discussed. Further, the earlier works on arithmetic circuits namely, full adder and compressor are explained. In addition, the existing implementations of parallel adders and the necessary improvements on their architecture are given. Also, the existing works relating Full Adder are discussed. Finally, the existing hierarchy multiplier architecture and its associated drawbacks are discussed.

2.1 Survey of Literature

In [1] authors proposed a reduction of delay, leakage current, leakage power. First find out the leakage current and leakage power. Which uses a gate diffusion input technique. By using this no of transistor is reduced. If the number of transistors is reduced, area is also reduced, leakage current also affected. To study all parameters in this thesis uses a 2x1 MUX, 4x1MUX,16x1 MUX and Full Adder. Applying a GDI technique and implemented by using a CMOS technique. Then do comparisons on GDI and CMOS technique and do a capacitance calculation. To implement all those things, use a microwind 3.1 and EDA 2.0. It is an Electronic Design Automation (EDA) environment that allows implementing a integrating in a single framework different applications and tools, allowing supporting all the stages of IC design and verification from a single environment. The resulting layout must verify some geometric rules dependent on the technology (design rules). Now checked with a Design Rule Checker (DRC) to find any error in the layout diagram and then simulation is performed. In implementing and do a comparison of GDI and CMOS technique.

In [2] authors proposed the Full Adder is a one of the most basic operational units in any processor. The Full Adder can be defined as the combinational unit which is used to perform its logical and arithmetic units. This paper presents a low power high speed Full Adder (Full Adder) in 14 nm technology using multi-threshold voltage transistor logic and Gate Diffusion Input technique. Its performance is compared with conventional CMOS technique. The simulated results revealed better

performance characteristics of various arithmetic and logic functions of a 1-bit Full Adder using MTV and GDI techniques compared to conventional CMOS technique. This technique allows reducing power dissipation and delay while maintaining low complexity of logic design.

In [3] authors proposed the design of an 8-bit Full Adder using Gate Diffusion Input (GDI) technique is proposed. Implementing the GDI technique in designing the Full Adder results in low power consumption and the number of transistors it requires is much less. Which result in reduced chip-area and power consumption - two of the most important parameters in digital VLSI design. In this design, 3T XOR is used in the full adder. Moreover, a novel 1-to-8 demultiplexer circuit has been used in the design as well. A considerable number of research papers are studied and compared various logic families and then finally designed an 8-bit Full Adder which can perform 8 different operations.

In [4] authors proposed a reduction of delay, leakage current, leakage power. First find out the leakage current and leakage power. This thesis uses a gate diffusion input technique. By using this no of transistor is reduced. If number of transistors is reduced, area is also reduced, leakage current also affected. To study all parameters in this thesis uses a 2x1 MUX, 4x1MUX,16x1 MUX and Full Adder. Applying a GDI technique and implemented by using a CMOS technique. Then do comparisons on GDI and CMOS technique and do a capacitance calculation. To implement all those things, use a microwind 3.1 and EDA 2.0. It is an Electronic Design Automation (EDA) environment that allows implementing a integrating in a single framework different applications and tools, allowing supporting all the stages of IC design and verification from a single environment. The resulting layout must verify some geometric rules dependent on the technology (design rules). Now checked with a Design Rule Checker (DRC) to find any error in the layout diagram and then simulation is performed.

In [5] authors present an In-Memory Computation (IMC) architecture using Full Swing Gate Diffusion Input (FS-GDI) in a single-ended disturb-free 6T SRAM. Not only are basic boolean functions (AND, NAND, OR, NOR XOR2, XOR3, XNOR2) fully realized, a Ripple-Carry Adder (RCA) is also realized such that IMC is feasible without Full Adder (Arithmetic Logic Unit) or CPU. FS-GDI reserves the benefits of the original GDI, and further resolves the reduced voltage swing issue, but it leads to speed degradation and large static power. Therefore, by using in-memory computing techniques, the well-known von-Neumann bottleneck will be mitigated as well as energy efficiency is enhanced.

In [6] authors proposed the CMOS technology is continuously becoming smaller and smaller in nanoscale regimes, and circuit resistance to changes in the process for the design of the circuit is a major obstacle. Storage elements such as memory and flip-flops are particularly vulnerable to the change process. Power consumption is also another challenge in today's Digital IC Design. In modern processors, there are many transistors, more than a billion transistors, which increases the temperature and the breakdown of its performance. Therefore, circuit design with low power consumption is a critical need for integrated circuits today. In this study, we deal with GDI techniques for designing logic and arithmetic circuits. We show that this logic in addition to low power consumption has little complexity so that arithmetic and logic circuits can be implemented with fewer transistors. Various circuits such as adders, differentiation, and multiplexers, etc. have been designed and implemented using these techniques, and published in various articles.

In [7] authors proposed the digital integrated chip the multipliers are the basic module needed for almost all arithmetic and logic unit (Full Adder) application. It is used right from small multiplier circuits to huge multiprocessor design, hence since its uses are vast so the design needs to be very efficient with respect to its desired operation and also it should be capable for low power and high-speed operation. This paper presents 4X4 bit binary multiplier which uses half and full adder as its

circuit subsystems and to maintain low power and high speed the gate diffusion input (GDI) cells are used. The result shows the low power and high-speed operation of the 4 X 4-bit binary multiplier as the proposed design consumes approximately 9µW power with the propagation delay of nearly 18ns.

In [8] authors proposed the Full Adder is an essential building block in many applications such as microprocessors, DSP, and image processing, while power efficiency is a general concern in VLSI design. This paper presents Delay time optimization of 4-bit Full Adder designed using full-swing gate diffusion input (GDI) technique. Simulations were carried out in Cadence virtuoso using 65nm TSMC processes with a supply voltage of 1.2 volts and a frequency of 125 MHz, Simulation results revealed improvement in Delay time and overall Energy of the optimized Full Adder design.

In [9] authors proposed A Full Adder is a heart of the processor which performs arithmetic and logic operations. To increase the performance of the processor, low power Full Adder is designed in this paper. The major parameters to measure the performance of any VLSI circuit design are power consumption, area and logic delay. This paper presents the implementation of an 8-bit Full Adder with optimized power consumption and chip area using Gate Diffusion Input (GDI) Technique. The proposed Full Adder performs 26 different operations. The computation of proposed Full Adder is carried out in parallel, and the results are available at the same time using Multiplexer. The proposed schematics of 8-bit Full Adder is simulated using a schematic editor EDA and Tanner for chip level design.

In [10] authors proposed the Arithmetic and Logic Unit is the fundamental building block of almost all the digital devices. Full Adder is the heart of the Central Processing Unit (CPU) of the computer. It is generally used to perform arithmetic and logical operations in the device. Full Adder can perform arithmetic operations like addition, subtraction, multiplication, increment, decrement, shift operations, and logical operations like AND, OR XOR, NAND, NOR, etc. Any digital device has its characteristics; based on its characteristics Full Adder is configured. The parameters like the speed of operation, power, accuracy, etc., are taken care of during the design. This paper presents the design of 8-bit Full Adder which performs 16 operations in 45 and 90 nm technology and compares parameters like power and delay.

In [11] authors analyzed basic full adder circuitry, which is implemented using CMOS technology (28T) and GDI technique (10T) using 18nm FinFET technology. The primary objective is to optimize our conventional adder so that an experimental analysis is conducted in order to analyze these two distinct circuits with same operation in terms of Area, Propagation Delay, Power and Power-Delay-Product (PDP). All experimental analysis is carried using Cadence Virtuoso (cds-ff-mpt library is used for FinFET)

In [12] authors proposed the area and power efficient design of 8-bit Carry Select Adder (CSLA) has been proposed. Conventional and other CSLAs are designed using CMOS technology, which has complexity in terms of area and power consumption. So, to overcome this problem a new technology is implemented on the CSLA. This paper shows the implementation and comparison of Carry Select Adder (CSA) using BEC (Binary Excess one Converter) and First Zero Finding (FZF) logic implementation techniques with optimization of GDI Logic by minimizing number of transistors.

In [13] authors proposed the work main focuses on the design and implementation of efficient decoders due to vast requirement of decoders in security application and communication decrypting it has become essential circuit in today's application this work demonstrates the design of 2-4,4-16 decoders using conventional,gdi,mixe style of design this experiment shows that result of a decoder like 2-4 decoder implemented in all designs and we can see power dissipation decreased using gdi by

57% and delay by 72% than using of previous designs and complexity , area of decoder circuit is reduced

In [14] authors proposed the priority encoder finds its wide scope as microprocessor interrupt controllers in digital and computer systems, where they classify the highest priority input. A Priority level is assigned to every input. The currently active input that has the highest importance agrees well with the output. A proficient implementation of 4-bit priority encoder using the modified gate diffusion input technique has been proposed in this research work. A simulation was carried out using Cadence 180 nm technology comparison made with complementary CMOS and Modified Gate Diffusion Input technique quality test matrices. This technique is much higher in speed and is a technique with limited power consumption.

In [15] authors proposed the Circuit designing is an emerging field and as per the recent trend it evolves digital devices in use portable as well as smaller in size. This paper proposes two designs of full subtractor circuit based upon eight and nine transistors demonstrating low power consumption and high-speed switching. The combination of 3T XOR and modified gate diffusion input (M-GDI) technique has been implied to realize the circuits.

3. PROPOSED METHOD

3.1 Design of Gates using GDI Logic

The gates required for realizing any arithmetic function are AND, OR, XOR and XNOR. These gate functions can be achieved with two transistors (excluding the inverters for complementary input signals) and their transistor level diagrams are shown in Figure 4.1.

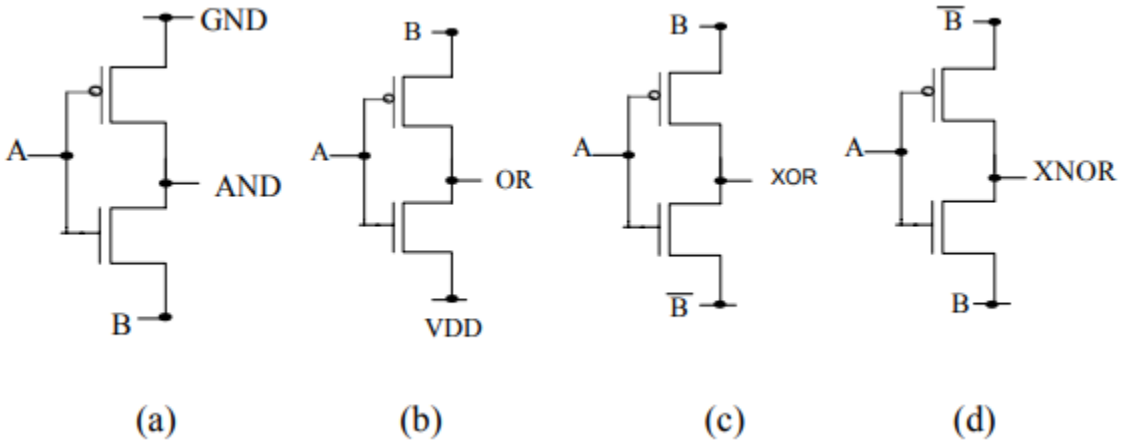

Fig. 1: GDI based gates (a) AND (b) OR (c) XOR and (d) XNOR.

The operational characteristics of these gates are given in Table 4.1. Assume both the inputs have voltage swing, then the output voltages are subjected to different input combinations as given in Table. 1.

Table. 1: Operational characteristics of gates using GDI logic.

INPUT		LOGIC GATE			
A	B	*AND*	*OR*	*XOR*	*XNOR*
'0'	'0'	$\|V_{tp}\|$	$\|V_{tp}\|$	$\|V_{tp}\|$	V_{DD}
'0'	'1'	$\|V_{tp}\|$	V_{DD}	V_{DD}	$\|V_{tp}\|$
'1'	'0'	*GND*	V_{DD}-V_{tn}	V_{DD}-V_{tn}	*GND*
'1'	'1'	V_{DD}-V_{tn}	V_{DD}-V_{tn}	*GND*	V_{DD}-V_{tn}

AND Gate: The transistor level diagram of the AND gate using GDI logic is shown in Figure 4.1 (a). The working mechanism of this gate is explained below:

- **Logic '0':** For the input combinations AB = 00 and 01, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output is approximately equal to |Vtp| is obtained at the output, where Vtp is the threshold voltage of PMOS transistor. However, when AB = 10, the NMOS transistor becomes ON and PMOS transistor becomes OFF and passes ground potential (GND) at the output.
- **Logic '1':** When AB = 11, NMOS transistor is switched ON and PMOS transistor is switched OFF. Due to its operational characteristics, it delivers poor '1' signal which is about VDD-Vtn at the output, Vtn denotes the threshold voltage of NMOS transistor.

OR Gate: The transistor level diagram of the OR gate using GDI logic is shown in Figure 4.1 (b). The working mechanism of this gate is explained below:

- **Logic '0':** When AB = 00, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output approximately equal to |Vtp| is obtained at the output.
- **Logic '1':** When AB = 01, PMOS transistor is switched ON and NMOS transistor is switched OFF. Therefore, VDD passes through PMOS transistor. On the contrary, the case occurs when AB = 10 and 11. In this case NMOS turns ON and PMOS turns OFF resulting in poor '1' signal in NMOS which is about VDD-Vtn at the output.

XOR Gate: The transistor level diagram of the XOR gate using GDI logic is shown in Figure 4.1 (c). The working mechanism of this gate is explained below:

- **Logic '0':** When AB = 00, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output obtained is approximately equal to |Vtp|. However, when AB = 11, the NMOS transistor becomes ON and PMOS transistor becomes OFF and passes ground potential (GND) at the output.
- **Logic '1':** When AB = 01, PMOS transistor is switched ON and NMOS transistor is switched OFF. Therefore, VDD passes through PMOS transistor. On the contrary, the case occurs when AB = 10. In this case NMOS turns ON and PMOS turns OFF resulting in poor '1' signal in NMOS which is about VDD-Vtn at the output.

XNOR Gate: The transistor level diagram of the XNOR gate using GDI logic is shown in Figure 4.1 (d). The working mechanism of this gate is explained below:

- Logic '0': When AB = 01, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output is approximately equal to |Vtp|. However, when AB = 10, the NMOS transistor becomes ON and PMOS transistor becomes OFF and passes ground potential (GND) at the output.

- Logic ‘1’: When AB = 00, PMOS transistor is switched ON and NMOS transistor is switched OFF. Therefore, VDD passes through PMOS transistor. On the other hand, when AB = 10, NMOS turns ON and PMOS turns OFF resulting in poor ‘1’ signal in NMOS which is about VDD-Vtn at the output.

From this discussion, it is concluded that the output voltages are degraded by threshold voltage drop for certain input combinations. The reduction in output voltage increases significantly with increase in number of stages. Therefore, the design of full swing gates is necessary and it is discussed in the forthcoming subsections.

3.2 Proposed Full Adder

The GDI design technique was introduced as a promising alternative to the CMOS logic design style of complimentarily functioning gates. Originally proposed for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes, GDI methodology allows the implementation of a wide range of complex logic functions using merely two transistors. GDI implementation of a design thus helps in reducing its overall transistor count and thereby improves area constraints of the design.

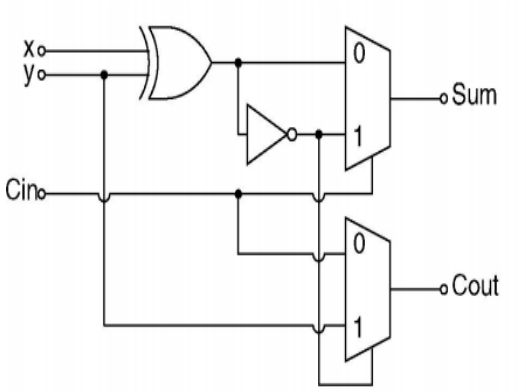

Fig. 2: Block diagram of proposed GDI full adder.

Full adders are the basic building blocks in every integrated circuit; thus, the design and development of the full adder must be done carefully. The conventional CMOS based full adders consume the higher power, delay and energy consumption values. Hence, the FinFET and GnrFET technologies are the alternative technology for the fundamental CMOS technology, which supports the low resource utilization. This section deals with the detailed implementation of full adder using FinFET and GnrFET technologies with 10T modelling. Figure 4 presents the block diagram of the proposed full adder, which shows the detailed operation of one bit addition using various components such as XOR, NOT gates and Multiplexer 2 to 1(MUX21), respectively.

The operations of the proposed FA are mainly focused on MUX21 switching operations. Here, the computational complexities of the MUX21 are very low, because its performance the fast triggering of data compared to other building blocks. Further, this triggering operation also satisfies the logic of FA.

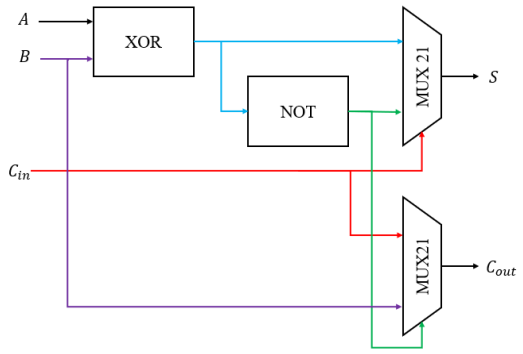

Fig. 3: Block diagram of proposed full adder.

Initially, inputs A, B are applied to the XOR gate, which generates the half adder sum output, and this outcome is applied as data input (input 0) to the MUX21. Further, the XOR gate is applied to the NOT gate, which generates the outcome as XNOR, respectively. In addition, XNOR outcome is applied data input (input 1) to the MUX21 with C_{in} as its selection input, respectively. Moreover, MUX21 selects the data inputs between XOR and XNOR outcomes based on C_{in}, which is illustrated by using following equation (3) and equation (4), respectively. The sum (S) of full adder is illustrated in equation (2) as follows:

$$\mathrm{S} = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C_{in}} \quad (2)$$

$$\mathrm{C_{in}} = 0 \rightarrow \mathrm{S} = \mathrm{A} \oplus \mathrm{B} \oplus 0 \rightarrow \mathrm{A} \oplus \mathrm{B} \quad (3)$$

$$\mathrm{C_{in}} = 1 \rightarrow \mathrm{S} = \mathrm{A} \oplus \mathrm{B} \oplus 1 \rightarrow \mathrm{A} \odot \mathrm{B} \quad (4)$$

Similarly, XNOR outcome is applied as selection input to the second MUX21 with C_{in} as "data input 0" and B as "data input 1" and generates the carry out (C_{out}), respectively.

Further, Equation 5 shows the basic operation of full adder carry out and it is remodified according to the XOR-XNOR logic for multiplexer-based implementations.

$$\mathrm{C_{out}} = AB + C_{in}(A \oplus B) = C_{in}(A \oplus B) + \bar{B}(\mathrm{A} \odot \mathrm{B}) \quad (5)$$

Further, equation (6) and equation (7) explain the process of carry out generation as follows:

$$\mathrm{A} \odot \mathrm{B} = 0 \rightarrow \mathrm{C_{out}} = \mathrm{C_{in}} \quad (6)$$

$$\mathrm{A} \odot \mathrm{B} = 1 \rightarrow \mathrm{C_{out}} = \mathrm{B} \quad (7)$$

The operational implementation of these equations is indicated by the various colors.

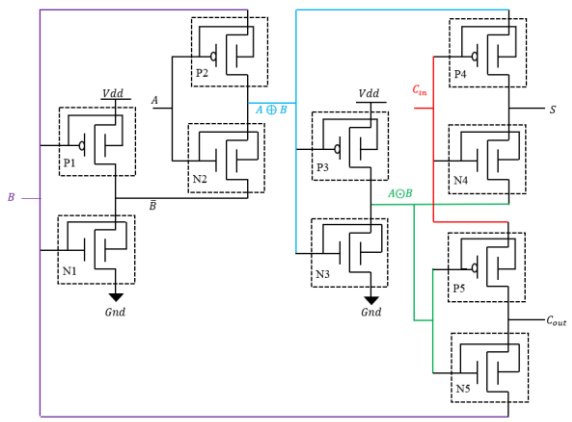

Fig. 4: FinFET modelling of proposed full adder.

FinFET modelling of the proposed full adder, which consist of 5 number of FinFET PMOS transistors and 5 number of FinFET NMOS transistors, respectively. Here, both the PMOS and NMOS transistors are equal, which makes to introduce the equilibrium state in proposed full adder, so the un-biased electron-hole pair will be controlled and synchronized.

Table. 2: Proposed full adder operational table.

Inputs			Sum Output	Comments for sum	Temporary outcome	Carry out outcome	Comments for carry out
C_{in}	A	B	S		XNOR (A, B)	C_{out}	
0	0	0	0	Eq. (3) is indicated by blue color	1	0	Eq. (6) is indicated by red color
0	0	1	1		0	0	
0	1	0	1		0	0	
0	1	1	0		1	1	
1	0	0	1	Eq. (4) is indicated by green color	1	0	Eq. (7) is indicated by violet color
1	0	1	0		0	1	
1	1	0	0		0	1	
1	1	1	1		1	1	

Further, this equilibrium condition also maintains the optimal power consumption with improved energy efficiency. The combination of P1 and N1 FinFET transistors are act as inverter and they generate the outcome as $\bar{B}$ for the input B. Then, the combination of P2 and N2 FinFET transistors are act as XOR gate with $\bar{B}, A$ as inputs and generates the $A \oplus B$ output.

Table. 3: Proposed algorithm.

Inputs: A, B, C_{in}

Outputs: S, C_{out}

If (C_{in}==0)

$S = A \oplus B$

else

$S = A \odot B$

If $A \odot B$ ==0)

$C_{out} = C_{in}$

else

$C_{out} = B$

Further, the combination of P3 and N3 FinFET transistors are act as inverter and they generate the XNOR outcome as $A \odot B$ for the XOR input $A \oplus B$. In addition, the combination of P4 and N4 FinFET transistors are act as MUX21 with C_{in} as selection input, data input-0 as $A \oplus B$, data input-1 as $A \odot B$ and generates the sum output as S. Finally, the combination of P5 and N5 FinFET transistors are also act as MUX21 with $A \odot B$ as selection input, data input-0 as C_{in}, data input-1 as B and

generates the carry output as C_{out}, respectively. The same transistor level circuit is used for GnrFET based full adder implementation with the same operation.

4. RESULTS

Fig. 5 represents the timing diagram of proposed full adder, which consisting of A, B, CIN as inputs and SUM, COUT as the outputs, respectively.

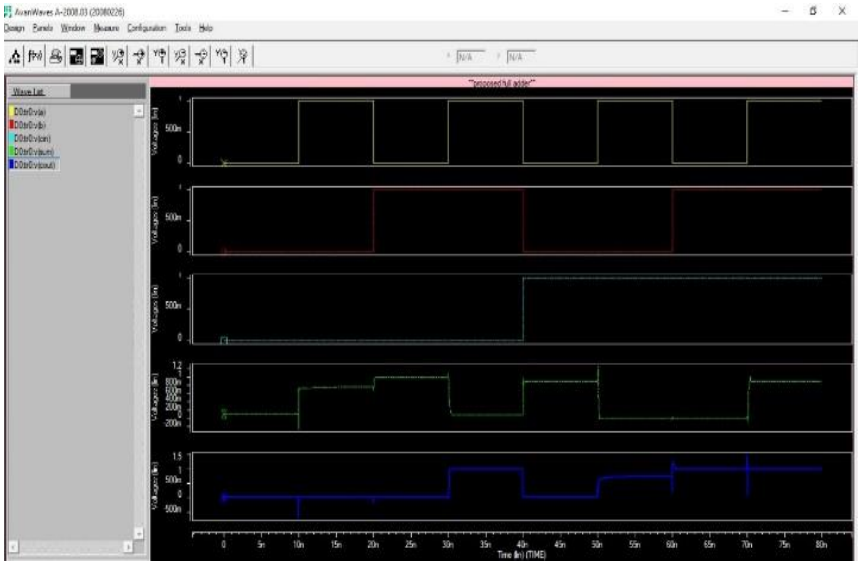

Fig. 5: Simulation outcome.

Fig. 6 shows the proposed full adder performance estimation. he provided information appears to be the results of a transient analysis for a proposed full adder circuit. Here's an explanation of each parameter:

- Average power consumption (nw): This represents the average power consumed by the full adder circuit during operation, measured in nanowatts. In this case, the average power consumption is 1.1200 nw.
- Sum rise delay (ns): It indicates the time it takes for the sum output to transition from a low to high voltage level. In this analysis, the rise delay for the sum output is 8.10002 ns.
- Sum fall delay (ns): This parameter represents the time it takes for the sum output to transition from a high to low voltage level. The fall delay for the sum output is 10.2315 ns.
- Cout rise delay (ps): It denotes the time delay for the carry-out (Cout) output to transition from a low to high voltage level. The rise delay for the Cout output is 1.0106 picoseconds (ps).
- Cout fall delay (ps): This indicates the time delay for the Cout output to transition from a high to low voltage level. The fall delay for the Cout output is 8.0846 ps.
- Propagation delay (ns): It represents the time it takes for the outputs (sum and Cout) to stabilize after a change in the inputs. The propagation delay in this case is 1.0026 ns.
- Total current (nA): This parameter indicates the total current flowing through the circuit during operation, measured in nanoamperes. The total current is 1.3059 nA.
- Static power (nw): It represents the power consumed by the circuit when there are no changes in the inputs. In this case, the static power consumption is 1.0447 nw.

- Total energy (nJ): This parameter denotes the total energy consumed by the circuit during operation, measured in nanojoules. The total energy consumption is 0.0372 nJ.
- Static noise margin: It is a measure of the robustness of the circuit and represents the voltage difference between the input levels that can be correctly interpreted as a valid logic level. In this case, the static noise margin is 3.0000, indicating a significant margin for reliable operation.

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******
**proposed full adder**
 ******  transient analysis                tnom=  25.000 temp=  25.000
******


Average power consumption (nw)= 1.1200 from=  0.0000E+00     to=  2.0000E-07
Sum rise delay (ns)     =8.10002 from=  5.0000E-09     to=  2.0000E-07
Sum fall delay (ns)     =10.2315  targ=  4.0015E-08   trig=  4.0018E-08
Cout rise delay (ps)=   1.0106 targ=  1.0023E-08   trig=  3.0122E-08
Cout Fall delay (ps)=   8.0846 targ=  2.0007E-08   trig=  4.0008E-08
Propagation delay (ns)= 1.0026 targ=  1.0014E-08   trig=  4.0018E-08
Total current (nA)=     1.3059 from=  5.0000E-09     to=  2.0000E-07
Static power (nw)       =1.0447
total energy (nJ)       =0.0372
Static noise margin     =3.0000
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Fig. 6: Proposed full adder performance estimation.

5. CONCLUSIONS

In this study, we dealt with the simulation of different dynamics logic circuits, compared their results, and then offered a circuit for reducing power consumption. We saw that using the proposed buffer circuit power consumption was reduced sharply and its delay was lower. In the next level, we designed logic circuits in GDI techniques and designed logic circuits such as AND, OR, XOR and multiplexer with this technique. It was observed that this technique with fewer number of transistors, one can design logic circuits. Then we dealt with designing collector circuit with this technique and offered a collector circuit using this technique. With examining the foregoing, we concluded that the proposed circuit compared to the previous works has much less delay and power consumption.

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