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An Improved and More Space-Efficient MAC Unit for Computers Based on Vedic Arithmetic

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Abstract:
Using the urdhva tiryaghbhyam algorithm and compressor from Vedic mathematics, this work focuses on the efficient design of low power arithmetic circuits such fast adders and multipliers. As the use of computers and signal processing grows, so does the need for fast processing. In many real-time signal and image processing applications, higher throughput arithmetic operations are crucial to achieve the needed performance. It has been of interest for decades to create fast adder and multiplier circuits, since these arithmetic operations are among the most important in such applications. One efficient and low-power multiplier is based on Vedic mathematics. Using this method in calculation algorithms will lessen the load on the system in terms of complexity, execution time, power consumption, etc. From which high-end digital circuits like the MAC unit and the FIR filter are constructed and analysed for efficiency in terms of both space and processing speed. Every digital signal processor has a media access control (MAC) unit, which is a basic building element in computers and is employed in many real-time signal processing modules. Multiplier, adder, and accumulator make up the MAC's core components. In digital signal processing, the MAC unit is responsible for performing complicated and continuous operations through repeated multiplication and accumulation. One of the primary considerations for facilitating quicker responses in real-time signal-processing applications is the design of an efficient MAC unit.
Keywords: low power arithmetic circuits, Multiply and Accumulate, Digital Signal Processor (DSP), real time signal processing

Introduction

For computationally demanding real-time applications like video compression, gaming, graphics, etc. in today's digital age, VLSI design has prioritised speed and power optimisation. Our computing and entertainment needs must be met by low-power semiconductor ICs that effectively combine several complicated signal processing modules and graphics processing units. The VLSI chip designer is responsible for overcoming technical challenges such as speed and power consumption in consumer electronics, healthcare devices, aerospace vehicles, and manufacturing machinery. Battery life may be increased and power consumption decreased by strategically including low-power components in the design of the device's architecture. Microelectronic circuits designed with ultra-low power dissipation are in high demand due to the expanding market for portable, battery-powered electronic devices (such as mobile phones, game consoles, etc.). Power optimisation allows for several levels of abstraction to be reached. One of the primary tasks in today's digital age is to increase levels of integration and the demand for mobility by limiting the low power consumption and improving the speed of the circuits in a broad range of applications. Better performance in real-time applications may be attained by the careful

selection of an architecture that optimises both speed and low power consumption. Better performance may be achieved by the efficient design of arithmetic circuits, which can maximise speed for general purpose applications or throughput for signal processing applications. The complete adder is the backbone of every high-performance, low-power digital arithmetic circuit. Similar to how a FIR filter may be used to filter out undesired signals in real time applications, a digital frequency response can be implemented using a FIR filter. The output of these filters is then employed in a wide variety of signal processing applications. Typically, they are built using multipliers, adders, and a sequence of delays. Electrocardiography (ECG) is only one of many biosignal applications that need complex filters, therefore creating an effective Finite Impulse Response (FIR) filter is a significant challenge.

This study provides a brief overview of the use of noise filtering techniques to the area of electrocardiography (ECG) monitoring. Here, we investigate a potential new approach to continuous ECG monitoring that makes use of low-power, high-speed Digital Signal Processor (DSP) modules. By creating effective Finite Impulse Response (FIR) filters, the Electrocardiography (ECG) data is denoised and preprocessed. In this dissertation, an Urdhva tiryagbhyam algorithm is developed and analysed using Vedic mathematics, with a focus on designing an efficient compressor-based Multiply and Accumulate (MAC) unit and a FIR filter. The suggested designs are validated on a Virtex 5 FPGA using the XC5VLX110T device, and on a Spartan 6 FPGA using the XC6SLX100T-3FGG484 device, both utilising Xilinx 14.2 software.

Low power arithmetic design is crucial for improved performance and reliability in today's digital world. As power is dissipated, heat and higher temperatures reduce speed and reliability. Energy efficiency is a must for today's high-performance, portable electronic equipment. Increasing the market share of portable electronic devices necessitating the availability of low-power building blocks that allow the construction of long-lasting battery-operated systems. Arithmetic is the foundation of every other mathematical study. From simple counting to complex scientific and medical applications, signal processing (including FIR filters), and corporate computations, everyone uses Arithmetic, a term derived from the Greek word (arithmos). This has made the quest for a better and more rapid computer Arithmetic Unit a hot issue for decades. The addition is one of the most basic mathematical operations. Common mathematical procedures that rely on addition include subtraction, multiplication, division, and address computation. The full adder cell is the foundation of the binary adder, which improves the performance of the1-bit full adder that garnered so much attention (Vahid Foroutan et al., 2014), hence these operations find widespread usage in various VLSI applications. The arithmetic system is affected by the efficiency of adders, as addition, subtraction, multiplication, and division are the four operations of fundamental mathematics.

Digital arithmetic performance is profoundly affected by the logic style used in the circuit's construction. Many implementations of the microprocessor place the adder in the critical path

because it is a crucial component of arithmetic units like ALUs and multipliers. Digital signal processors in embedded systems where highprocessing-speed capabilities must deal with LP management have been the primary focus of research into specialised adders and arithmetic circuit topologies since the critical route dictates the total simultaneous system performance. One of the major cells in adders like carry select and carry-skip, as well as a ripple carry adder, is the 1-bit full adder, which may be modified to implement the carry propagation chain and increase the adder's performance. An n-bit RCA may be constructed using conditional sum adders (CSAs) or carry look-ahead (CLA) adders, both of which are fast adder designs that use just one bit of memory per addition. Researchers in both academia and industry have delved deeply into the many full adder types. Measures of performance include time, energy, and size. Mobile and embedded applications place a premium on low power consumption, hence it consistently ranks well in comparisons of circuit and system performance. Many of these variations of full adders aim to reduce the number of transistors required.

Vedic Mathematics

The word 'Vedic' is originated from the word 'Veda which means the store-house of all knowledge. 16 Sutras (or aphorisms) are the foundation of Vedic mathematics that deals with various branches of mathematics like arithmetic, algebra, geometry, etc. These Sutras along with their brief meanings are enlisted below alphabetically.

MAC And FIR Filters

Quick Filtering and Convolution One of the building blocks of Digital Signal Processing (DSP) applications like Fourier Transform (FFT) is the MultiplyAccumulate (MAC) block. Recent developments have seen the addition of a specialised Multiply Accumulate Unit (MAC unit) to general-purpose Microprocessors. The multiplier is located in the MAC unit's data stream and must function quickly and efficiently. Therefore, its function in the MAC unit is crucial. Combinational logic is used for the MAC unit's multiplier, which is accompanied by a fast adder and accumulator register to keep the results on the clock. Power efficiency and latency in digital systems may be reduced by careful optimisation at every stage of the design process. MAC is located in the system's last track, which is responsible for making the ultimate decision on the hardware's total speed and power. It is this calculation, Acc(N) = Acc(N-1)+Ai x Bi, that the MAC unit is primarily responsible for. The speed-power ratio of the MAC unit is dependent on the Partial Product Reduction Tree (PPRT) and the accumulator. PPRT is built out of adders and multipliers, whereas accumulators are created out of registers. To achieve optimal speed-power characteristics of the Multiply and Accumulator unit (MAC), the PPRT and accumulator units must be optimised.

Fast Adder Introduction

In today's rapidly expanding digital world, whereby portable electronic gadgets are limited by battery life. Increasing competition between integrated circuit designers and manufacturers

calls for the creation of high-performance circuits that need a minimal amount of chip space. In many DSP algorithms, the addition is the first and most essential step. The characteristics of chip area, power, and latency determine the overall performance of the system architecture. The adder is the backbone of several high-performance digital circuits, including multipliers, multiply-and-accumulate units, and FIR filter designs. This thesis proposes an efficient, quick adder that can be used to high-end arithmetic circuits utilised in many digital signal processing applications and enhances the overall system design performance in terms of latency. Since addition is the primary process in digital design, the speed of this operation will benefit the most complex calculations. The efficiency of the whole system design will increase thanks to the suggested fast adder architecture.

Array Multiplier Architecture The standard layout of an array multiplier is well-known. The multiplier circuit requires both shifting and adding operations. In order to get each partial product, it is helpful to multiply the multiplicand by a multiplier of one bit. By shifting and adding bits in the appropriate bit ordering, we may construct the partial products. The traditional array multiplier makes use of the complete adder cell. To save power and real estate, the standard array multiplier skips the last step of addition and feeds the carry bits into the input for the next column to the left. The products are typically added using carry save addition in a regular array multiplier. A full adder or a half adder may be found in the first row of this carry-sparing adding procedure. If complete adders are used to synthesise the first row of partial products, the input of Cin will be interpreted as 0. The forward carry of each full adder is sent to the following row of the half adder on the diagonal. The resultant multiplier is called a carry-save array multiplier because the carry bits are not added immediately but rather stored for the subsequent stage of addition of full adder. When designing complete adders, it's common practise to treat the third input as zero. Multiplier sums are subtracted before the carries are added using the last adder.

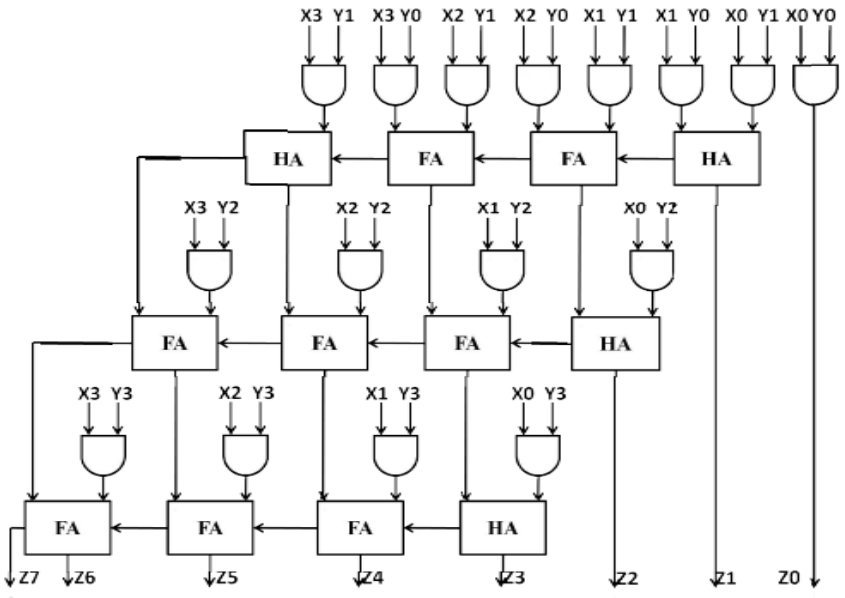

Figure 3 Array multiplier architecture

The last step involves adding the multiplier's inputs and carries together. The multiplier's carry from the fourth column is used as the input for the fifth column, rather than zero. For the same reason, the carry from the fifth column is fed into the sixth, and so on. The seventh column of an adder's carry determines the array multiplier's most significant bit (MSB).

Braun Multiplier Architecture

One of the array multipliers used for multiplying unsigned values is called a Braun's multiplier. The architecture of Braun's multiplier is made up of AND gates and complete adders. A 2-dimensional bypassing based multiplier is one in which the addition operations in the jth row or (i+1)th column may be skipped. In this case, if bits ai and bj are both zero and carry ci, j-1 is 1, neither row nor column by passing may be used to fix the output carry. Such a scenario calls for specialised bypassing circuitry. However, the ability to save power is diminished by the additional circuitry used. Bypassing methods are useful for lowering dynamic power consumption. If the multiplier bit bj is set to zero, the addition operations in the jth row are skipped, and the outputs from the jth row are sent straight to the j+1th row. That's why we're consolidating our electricity and switching operations. Exemplifying both the Braun Multiplier and Row Bypassing. Figure 4 depicts the hardware layout of a four-bit Braun multiplier. Here we have A0,A1,A2,A3, and B0,B1,B2,B4 as our two operands. Braun's approach yields a product known as P0-P7.

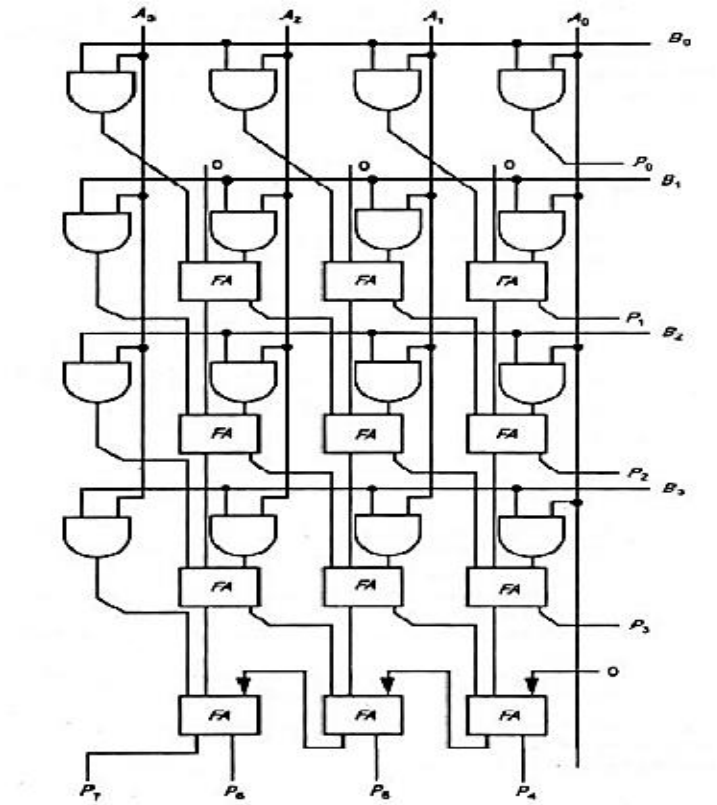

Figure 4. Braun array multiplier architecture

Literature Survey

K. Lilly et.al(2020) The Multiply and Accumulate (MAC) unit is the most common operation in digital signal processing. The efficiency and speed of an electronic system are significantly impacted by the MAC unit's footprint and power requirements. In this study, we present a 32-bit MAC with a vedic multiplier and ripple carry adder (RCA) and another MAC with a 32-bit array multiplier and RCA. In addition to the vedic multiplier and carry save adder, the paper includes a second modified MAC unit. ModelSim is used for simulation of all MAC components, while XILINX ISE DESIGN SUITE is used for synthesis. Space and time were compared across all MAC implementations. When compared to alternative MAC architectures, the delay introduced by the proposed design of MAC using vedic multiplier is minimal.

Aditi Chhabra et.al(2020) Artificial Neural Networks (ANNs) have been used to effectively resolve issues with machine learning. More substantial benefits may be attained by implementing neural networks on hardware. An essential operation in digital neural networks is the multiplication of weights by inputs. In this research, we compare and contrast many Vedic multiplier topologies with more conventional array multiplier configurations, and we also construct the MAC unit in hardware using VHDL. The MAC unit of ANN is dependent on routine arithmetic operations. The purpose of this comparison is to find an alternate method of realising the neural network's MAC unit. A network that employs the alternative multiplier in lieu of the standard array multiplier is also proposed in this research. The circuit shown in this research was designed specifically for the data used in the paper. The precision of the multiplier is taken into account to ensure the network's testing accuracy.

S. Swettha et.al., (2018) This article details the layout of a compact and power-saving multiplication and accumulation circuit. In DSP designs, the MAC is the central component. This component controls the system's total output and velocity. The future of Wireless sensor networks relies on the development of high-speed, low-power MAC. Vedic multiplier is utilised for quick multiplication, while Modified Gate Diffusion Input (MGDI) is employed to maximise power and minimise footprint. Before starting on the MAC unit design, we study each individual block and execute the entire layout in cadence virtuoso 45nm technology. The average amount of energy utilised is determined using the Cadence spectre software..

Monisha Yuvaraj et.al.,(2017) along most digital signal processing algorithms, multipliers are located along the crucial delay route and determine the algorithm's overall performance. Over the years, many methods have been proposed to lessen the burden on computers that traditional multipliers impose. One of them is the field of Vedic mathematics. In this study, we suggest a new multiplicator unit that takes the best features from all of the sutras and combines them into one. The "Sampoornam" alias "Absolute vedic" multiplier is built with a dedicated logic unit that, depending on the input types, chooses the most effective multiplier. A 4-bit Multiplier accumulator unit (MAC) unit may be designed with the help of the suggested multiplier Sampoornam, which can then be scaled up to 64 bits with the help of the Vedic scaling approach. When compared to modern multipliers like the (ab) algorithm, Booth, and Wallace, Sampoornam is much faster. The time delay of the 4-bit MAC unit

created with sampoornam is reduced by 25% as compared to the MAC created using the Wallace multiplier. The same pattern emerges as the number of bits grows.

Methodology

Better performance is achieved by combining the compressor based Vedic FIR (CVFIR) and Vedic multiplier (VMC) shown in Figure 5 with the CMCSA based adder. Many applications, including digital hearing aids, use real-time digital signal processing, which makes the FIR filter a crucial component. The suggested FIR filter is implemented and evaluated in this thesis for use with ECG biosignals.

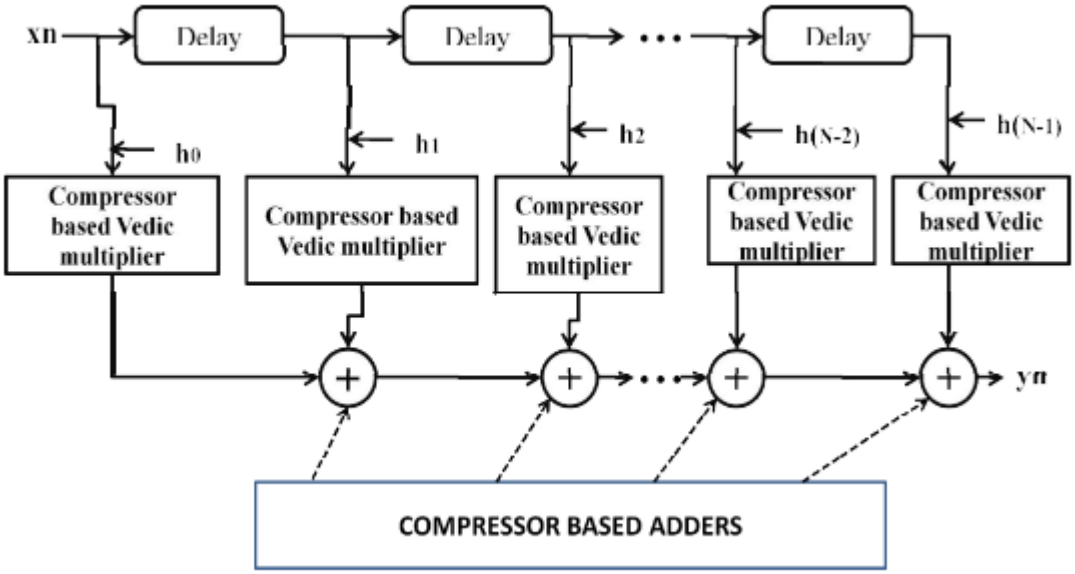

Figure 5. Proposed Vedic based FIR filter Architecture

Filter Design Analysis (FDA) Tool

Filter Design and Analysis Tool (FDATool) in MATLAB is a robust signal processing tool for studying digital filter. Setting filter performance parameters, importing filters from your MATLAB workspace, or explicitly defining filter coefficients or weighting factors all facilitate the creation of digital FIR or IIR filters using the FDATool. Phase response plots, magnitude plots, and pole-zero plots are all examples of how filters may be analysed using this method. The filter coefficients of a FIR filter are crucial for reducing noise in an input signal. Many real-time digital signal processing applications, such as Electrocardiography (ECG), rely on noise removal via FIR filters, and the FDA tool is used to generate the filter coefficients or weighting factors for designing the FIR filter. In this thesis, we create filter coefficients to attenuate power line noise at high frequencies in an electrocardiogram. The sampling frequency of 1000 Hz or 1 kHz with stop band attenuation may be used to filter out power line noise of 50 Hz from an electrocardiogram. Here, we normalise two frequencies, f1 and f2, to the Nyquist frequency of 500Hz, which is set at 1. Stop band variation for normalised 50Hz ranges between 0.07 and 0.13 for frequencies of 35Hz and 65Hz. The attenuation of the band is provided by 50/500, which is equal to 0.1. Filter coefficients or weighting factors for a 32-tap FIR filter are calculated using the filter design analysis tool

(FDA tool) in MATLAB's signal processing toolbox based on the aforementioned analysis settings.

Simulation Results

The proposed and existing architectures are developed using VHDL code and simulated using Xilinx ISE 14.2 tool.

Both the suggested Compressor-based Vedic FIR (CVFIR) and the Vedic Multiplier (VMC) with CMCSA Adder-based FIR have been simulated, with the results shown below.

Figures 5 and 6 exhibit the VHDL simulation output in binary and decimal formats, respectively, for the proposed compressor-based Vedic FIR (CVFIR) and the Proposed Vedic multiplier (VMC) with CMCSA adder-based FIR. Consider 'x' to be the 8-bit filter input, and 'yt' to be the filtered result. The coefficients of the 32-tap FIR filter are each 8 bits in size and are represented by the notation h0, h1, h2,..... h31. MATLAB's filter design analysis tool (FDA tool) in the signal processing tool box generates filter coefficients depending on the needs of the application.

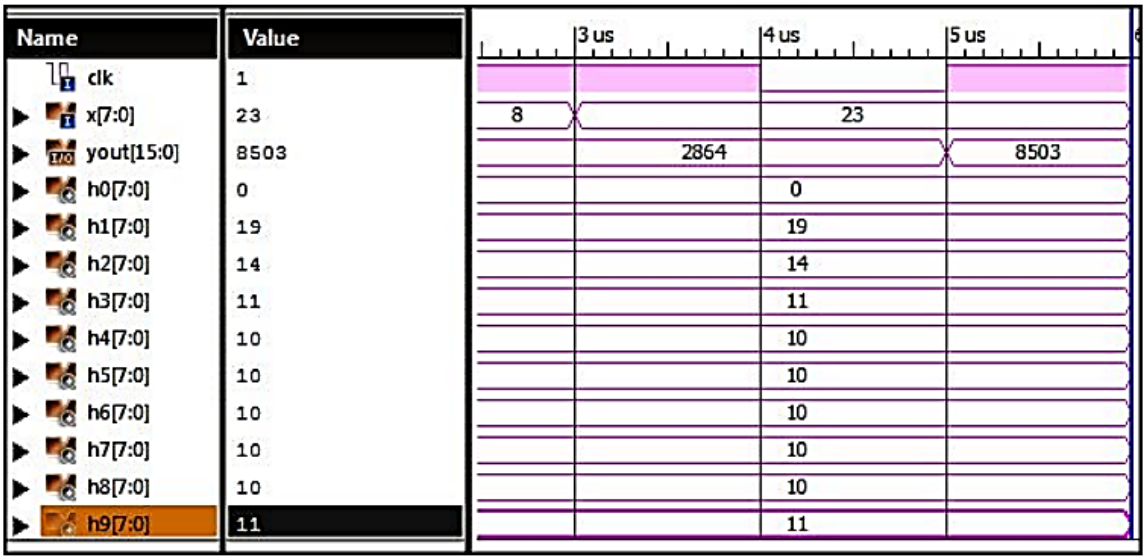

Figure 6 Simulation Output of proposed compressor based Vedic FIR (CVFIR) and Proposed Vedic Multiplier (VMC) with CMCSA adder based FIR in decimal format

Conclusion

When it comes to VLSI chip design, arithmetic circuits are a crucial component. In order for processors to carry out any task, low power high-speed arithmetic circuits are required. A growing number of digital signal processing (DSP) and general-purpose (GP) processors play pivotal roles in critical real-time applications. For real-time signal processing applications, we propose and construct high-end digital circuits based on Vedic principles, such as the Multiply and Accumulate (MAC) unit and FIR filter topologies.

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